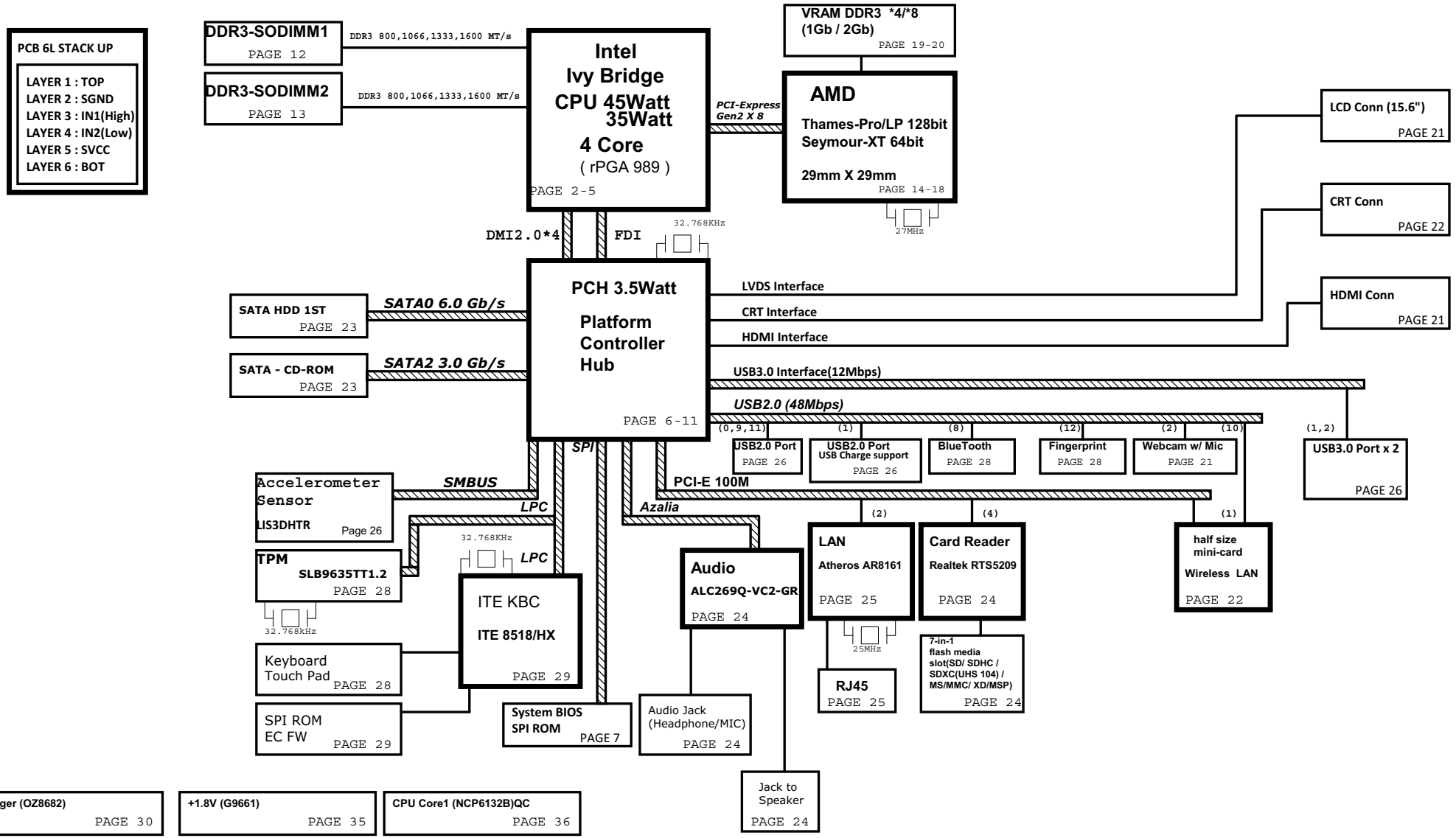
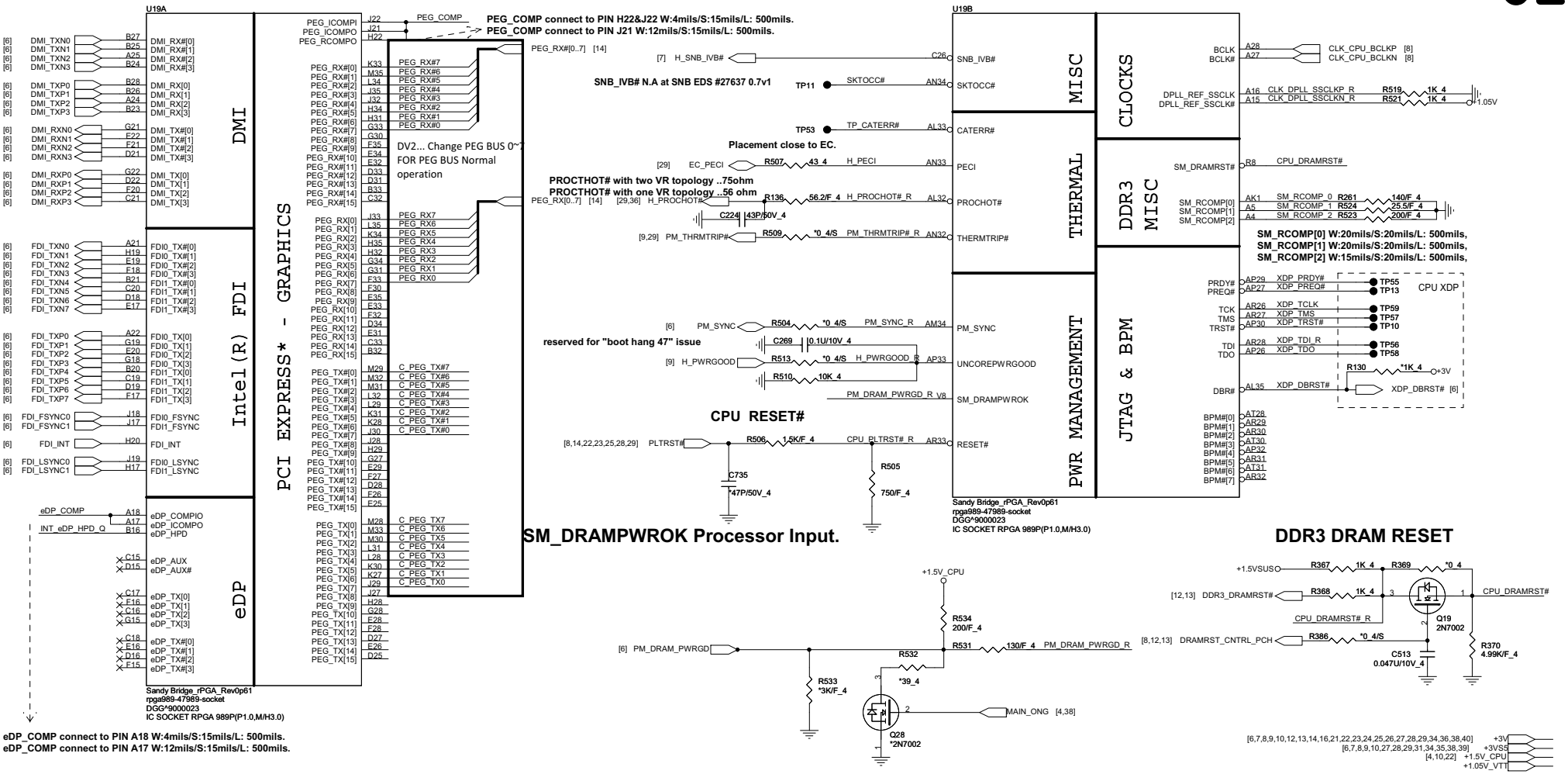
LG3/5 (14"/15.6") MUXLESS and UMA. BLOCK DIAGRAM 01



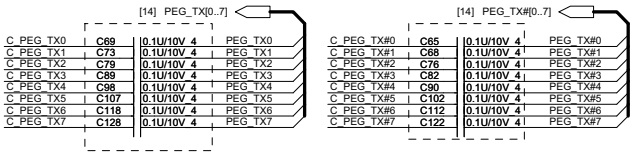
Sandy Bridge Processor (DMI,PEG,FDI)

Sandy Bridge Processor (CLK,MISC,JTAG)

02

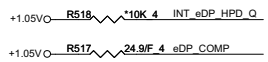


PEG x16 disable (UMA only remove)

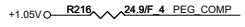


0.22uF AC coupling Caps for PCIE GEN1/2/3

DP & PEG Compensation



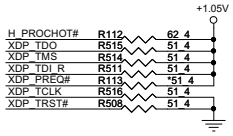
eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms



PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

Processor pull-up (CPU)

PROCTHOT# with two VR topology ..100ohm
PROCTHOT# with one VR topology ..62 ohm



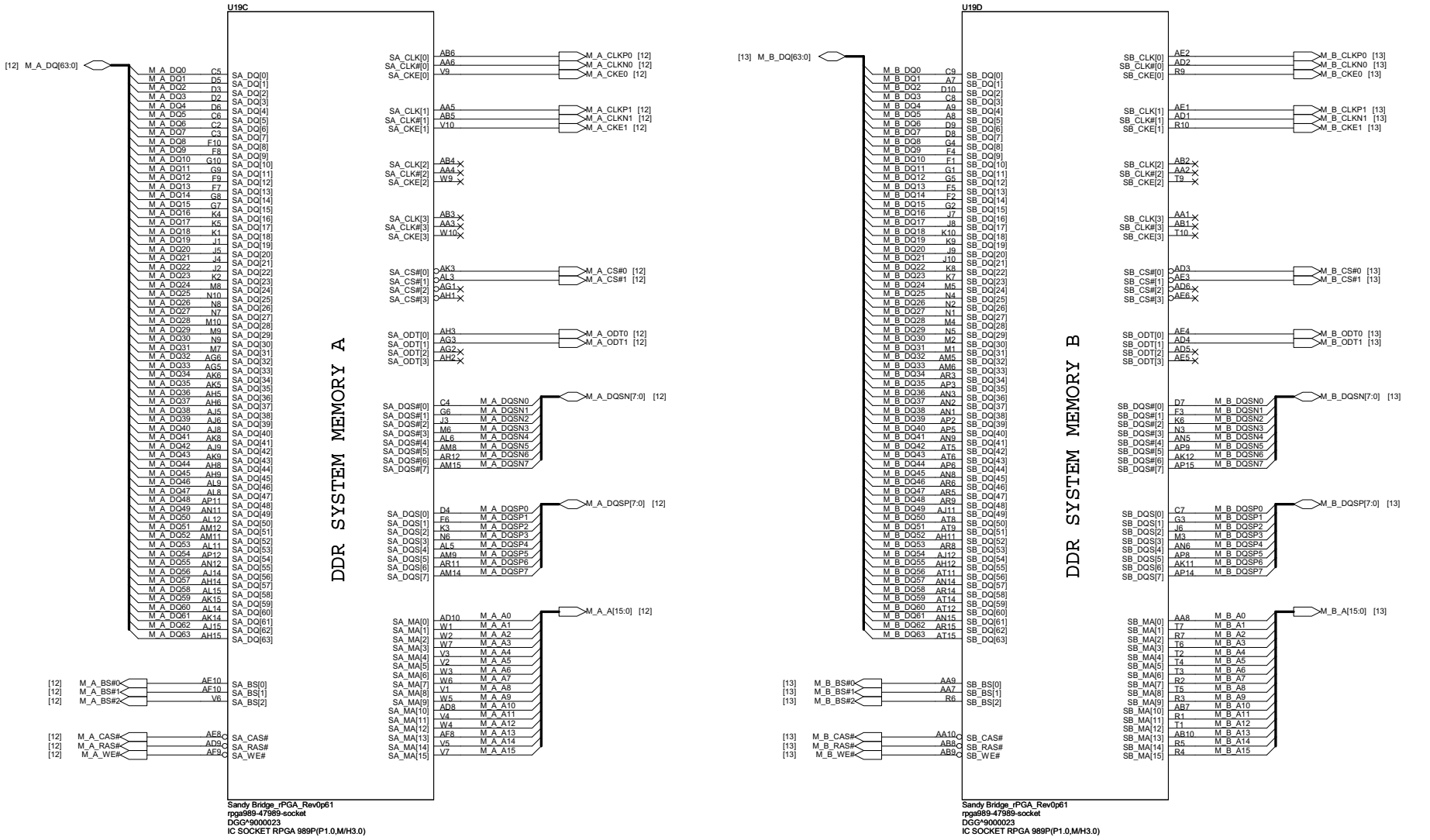
NB5

PROJECT : LG3/5 Muxless & UMA
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 1/4 (PCIE&DMI&FDI)	2A

Date: Wednesday, March 07, 2012 Sheet 2 of 42

Sandy Bridge Processor (DDR3)



PROJECT : LG3/5 Muxless & UMA
Quanta Computer Inc.

NB5

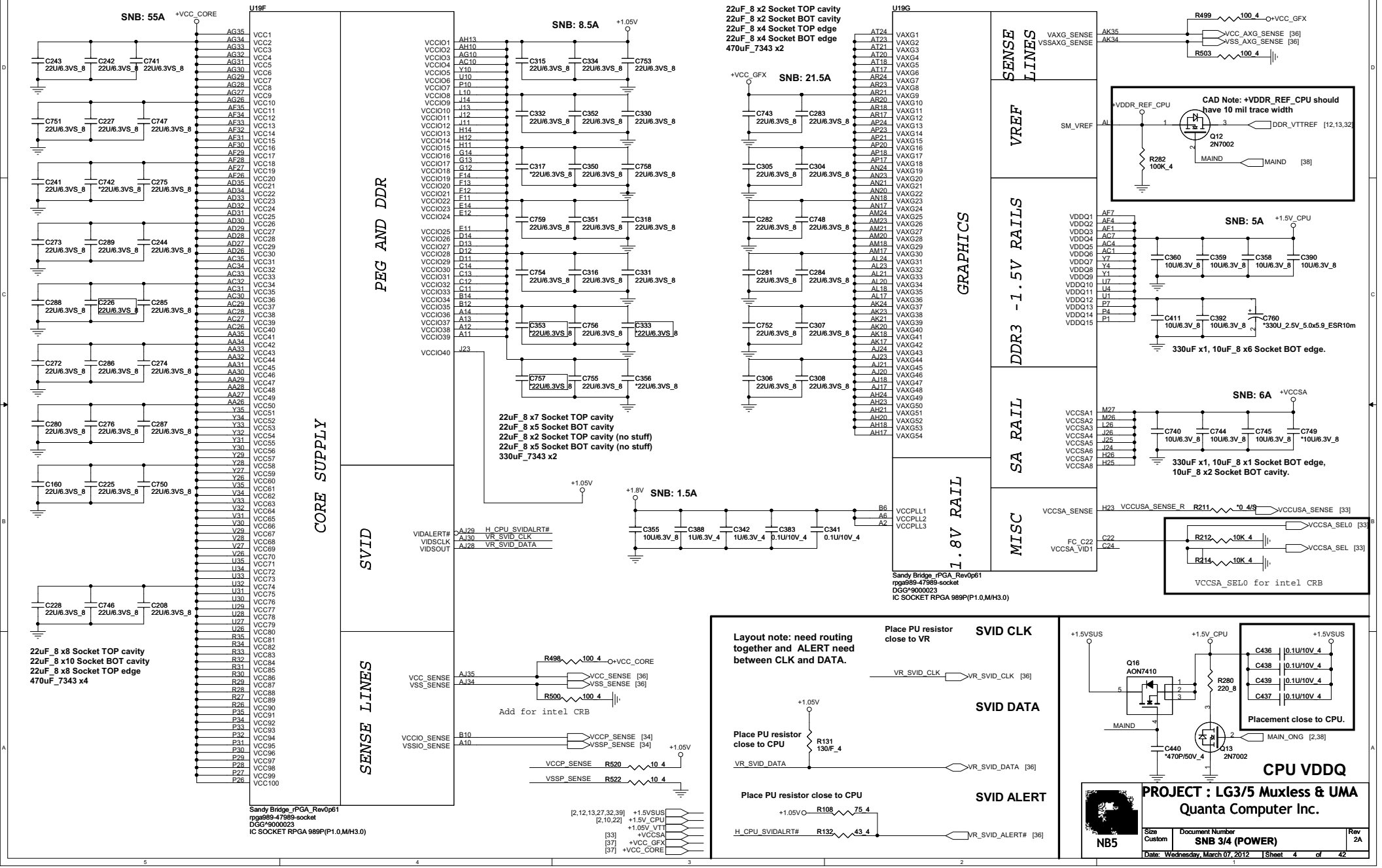
Size	Document Number	Rev
Custom	SNB 2/4 (DDR3 I/F)	2A

Date: Wednesday, March 07, 2012 | Sheet 3 of 42

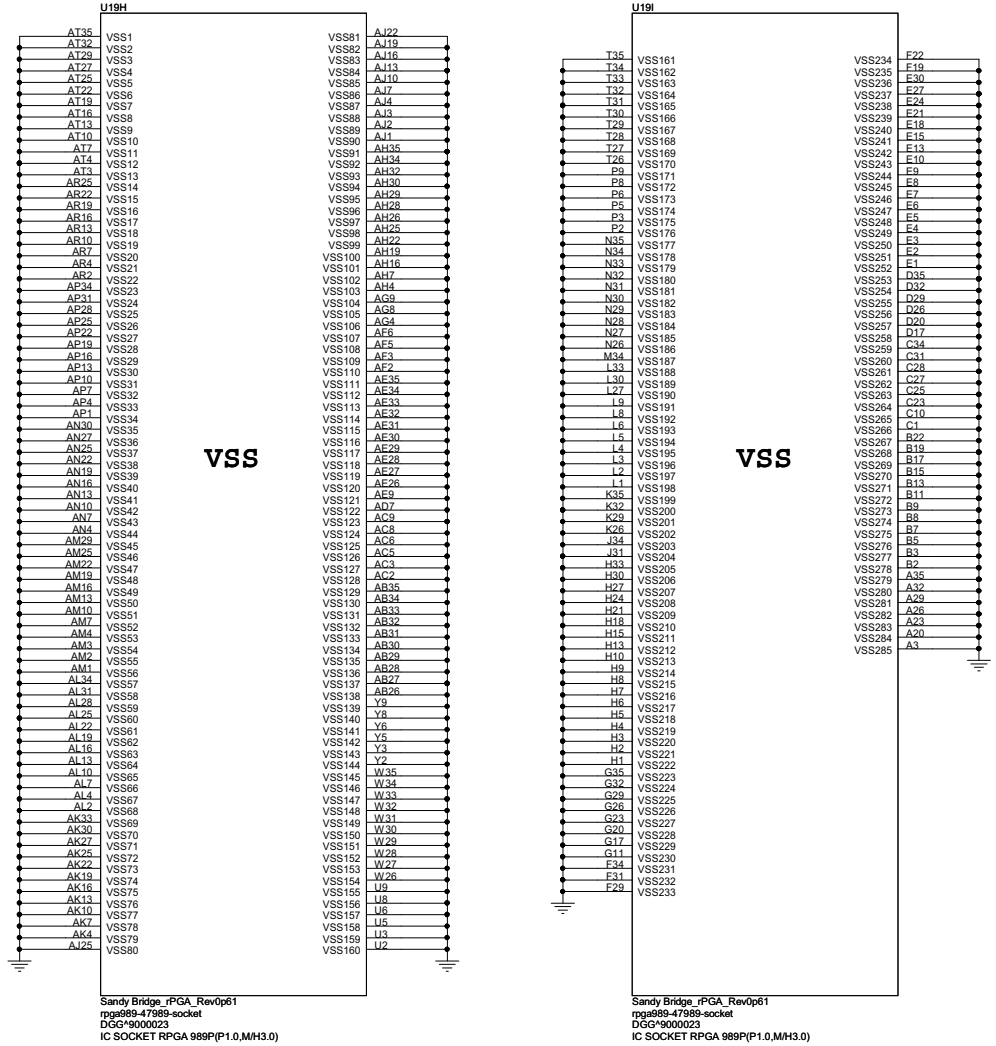
Sandy Bridge Processor (POWER)

Sandy Bridge Processor (GRAPHIC POWER)

04

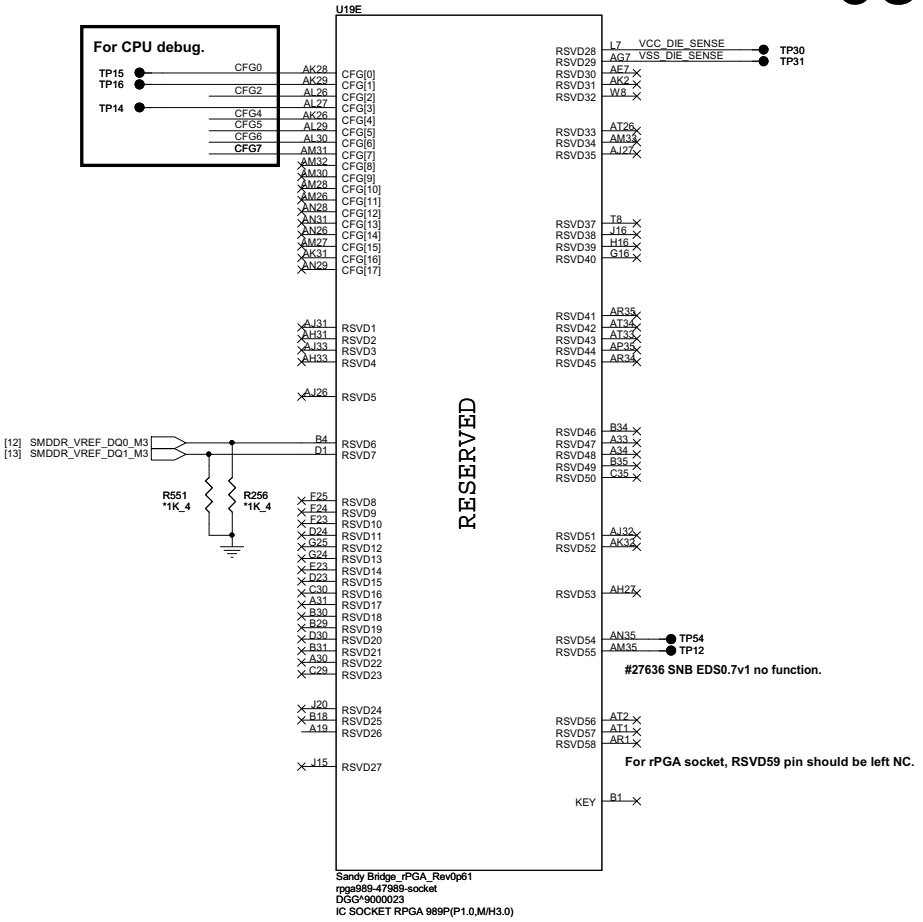


Sandy Bridge Processor (GND)



Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGQ*9000023
IC SOCKET RPGA 989P(P1.0,M/H3.0)

Sandy Bridge Processor (RESERVED, CFG)



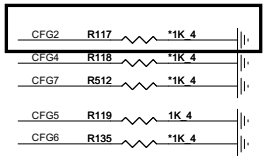
Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGQ*9000023
IC SOCKET RPGA 989P(P1.0,M/H3.0)

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

DV2...R117 NON-STUFF FOR PEG BUS Normal operation



CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

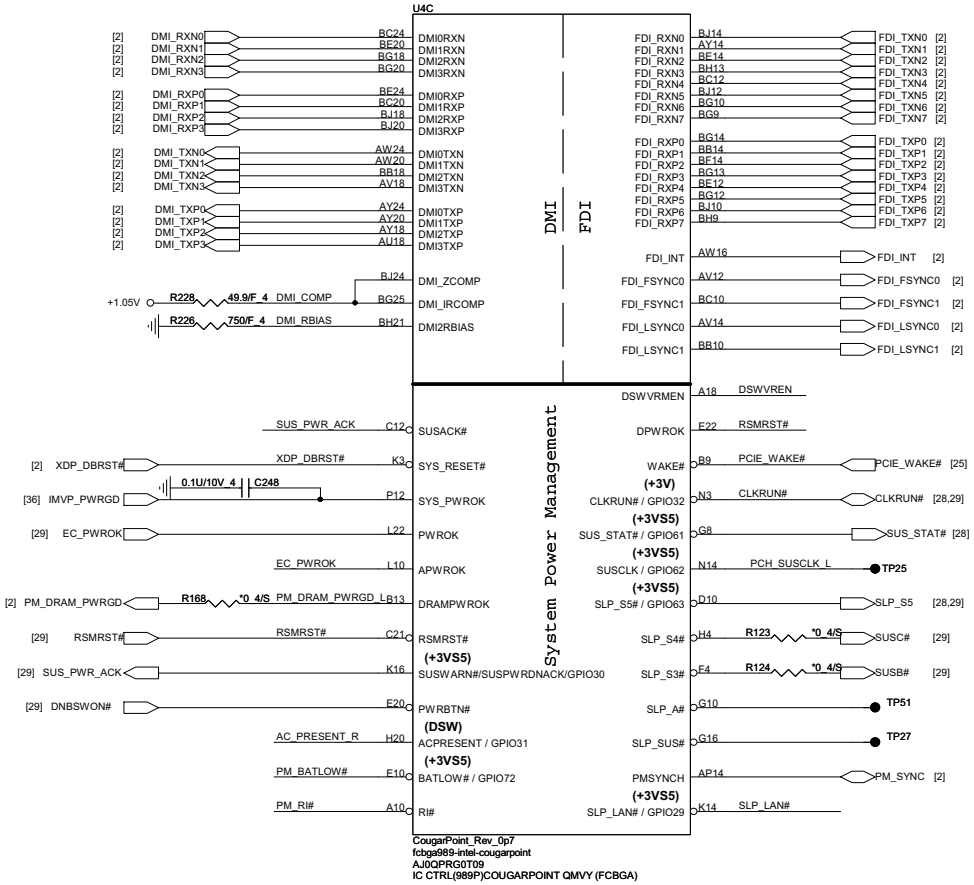
NB5

PROJECT : LG3/5 Muxless & UMA
Quanta Computer Inc.

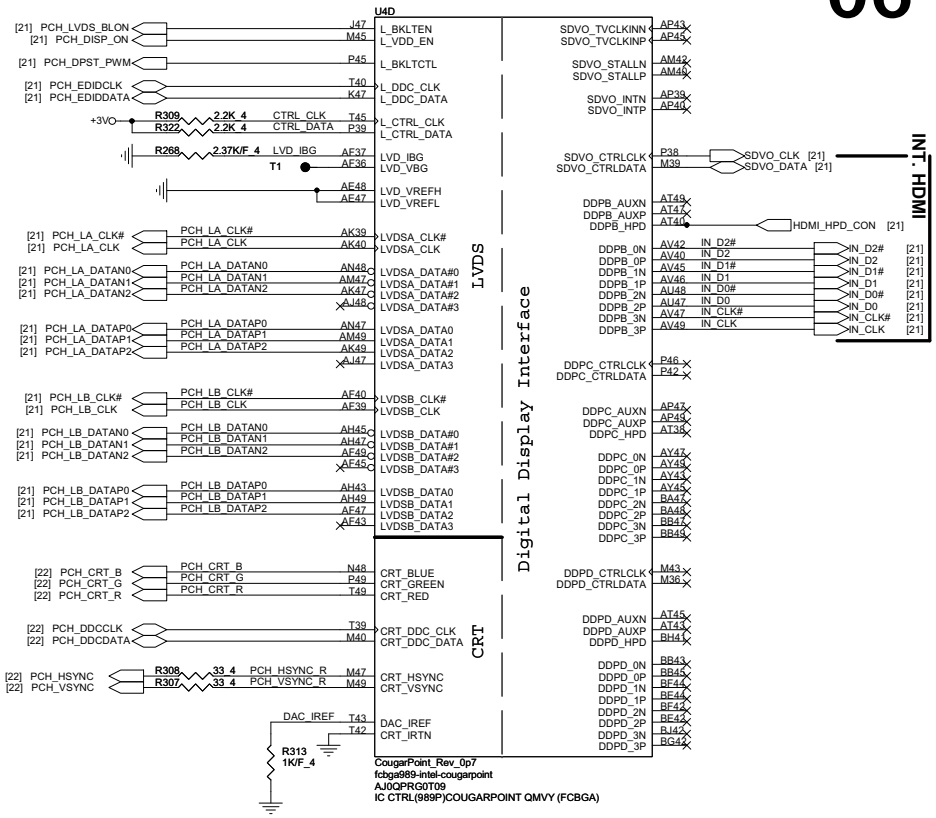
Size	Document Number	Rev
Custom	SNB 4/4 (GND)	2A

Date: Wednesday, March 07, 2012 Sheet 5 of 42

Cougar Point (DMI,FDI,PM)

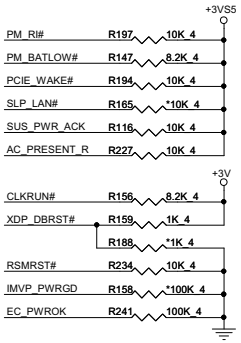


Cougar Point (LVDS,DDI)

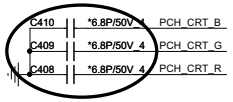


[7,10,21,22,23,24,26,28,38] +5V
[2,7,8,9,10,12,13,14,16,21,22,23,24,25,26,27,28,29,34,36,38,40] +3V
[7,8,9,10,27,28,29,31,34,35,38,39] +3VS5
[7,21,26,28,29,30,31] +3VPCU
[7,10,29] +3V_RTC
[2,4,7,8,10,29,34,36] +1.05V

PCH Pull-high/low(CLG)



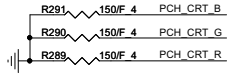
INT LVDS & CRT disable (DIS only remove)

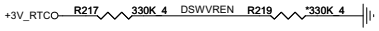


EMI(near PCH)

PD Res place close to PCH

PCH to Res routeing 50 ohm Impedance.
Res to connector filter routeing 37.5ohm Impedance.





On Die DSW VR Enable
High = Enable (Default)
Low = Disable

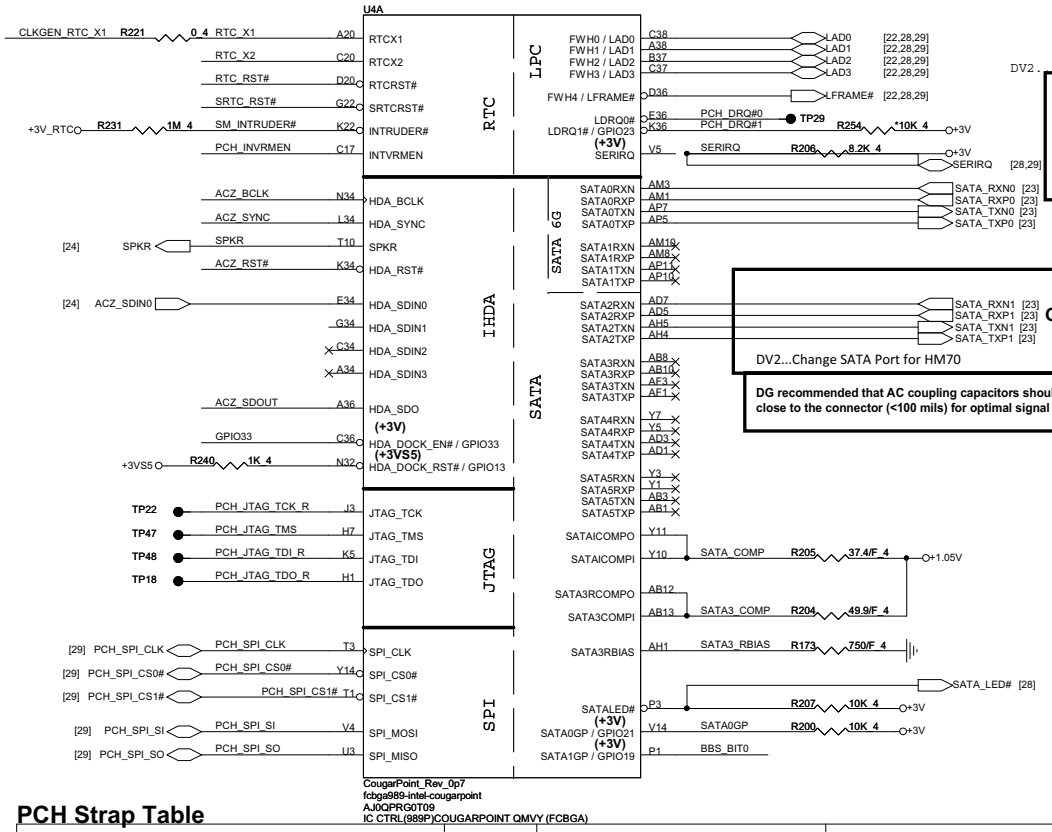
PROJECT : LG3/5 Muxless & UMA
Quanta Computer Inc.

NB5

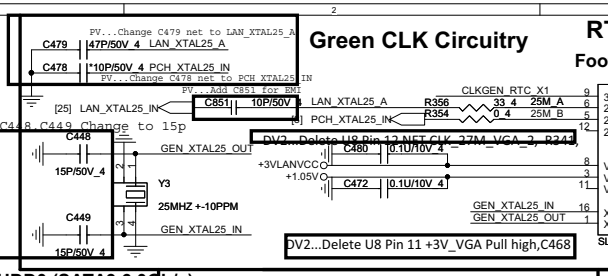
Size	Document Number	Rev
Custom	PCH 1/6 (DMI/FDI/VIDEO)	2A
Date: Wednesday, March 07, 2012	Sheet 6 of 42	

06

Cougar Point (HDA,JTAG,SATA)

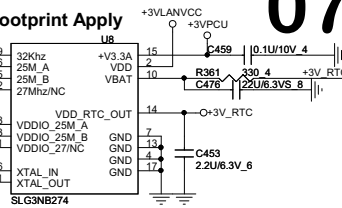


Green CLK Circuitry



RTC Clock 32.768KHz

Footprint Apply



07

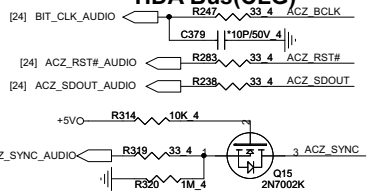
HDD0 (SATA3 6.0Gb/s)

ODD (SATA2,3Gb/s)

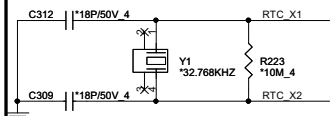
DV2...Change SATA Port for HM70

DG recommended that AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

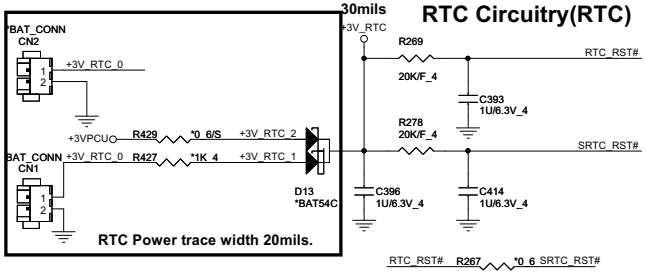
HDA Bus(CLG)



RTC Clock 32.768KHz



RTC Circuitry(RTC)



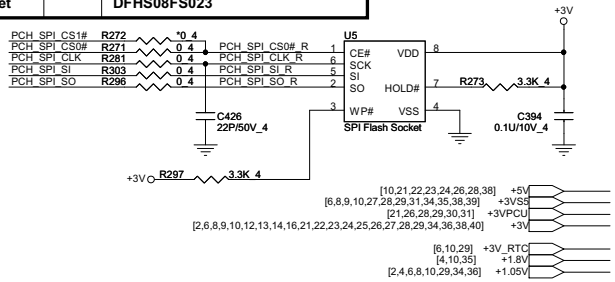
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR Different from Calpella	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	SPKR R175 *1K_4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R311 *1K_4, R324 10K_4, PCI_GNT3# [8]
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R218 330K_4 +3V_RTC
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R237 *1K_4 ACZ_SDOUT [29]
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# 1, GNT0# 1 → SPI GNT1# 0, GNT0# 0 → LPC	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#
GPIO19 Different from Calpella	Boot BIOS Selection 0 [bit-0]	PWROK		R181 *1K_4 BBS_BIT0, R286 *1K_4 BBS_BIT1 [8]
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V R171 *1K_4 NV_ALE [8]
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm	+1.8V R172 2.2K_4, R199 1K_4 NV_CLE [8], H_SNB_IVB# [2]
HDA_SYNC	**On-Die PLL VR Voltage Select**	**RSMRST**	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3VS5 R304 1K_4 ACZ_SYNC
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	[29] ACZ_SDOUT ACZ_SDOUT R239 *1K_4 +3VS5
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	R196 *1K_4 ICC_EN# [9]
GPIO28 Different from Calpella	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R157 *1K_4 PLL_ODVR_EN [9]
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	PCH_SPI_SI R203 1K_4 +3V

U5 Placement TOP side

Vender	Size	P/N
EON	2MB	AKE38ZN0Q00 (EN25QH16-104HIP)
AMIC	2MB	AKE38ZN0802 (AMIC A25LQ16M-F/Q)
Socket		DFHS08FS023

PCH SPI ROM(CLG)



NB5

PROJECT : LG3/5 Muxless & UMA
Quanta Computer Inc.

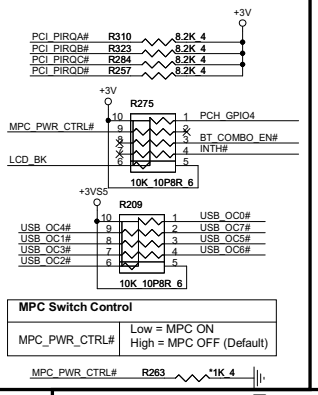
Size: Custom | Document Number: PCH 2/6 (SATA/HDA/SPI) | Rev: 2A
Date: Wednesday, March 07, 2012 | Sheet 7 of 42

Cougar Point-M (PCI,USB,NVRAM)

Cougar Point-M (PCI-E,SMBUS,CLK)

08

PCI/USBOC# Pull-up(CLG)



MPC Switch Control

MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)

MPC_PWR_CTRL# R263 *1K_4

USB3.0

[26] USB30_RX3- / USB30_RX4-
[26] USB30_RX3+ / USB30_RX4+
[26] USB30_TX3- / USB30_TX4-
[26] USB30_TX3+ / USB30_TX4+

DV2...Change USB3.0 Port for HM70

U4E

TP1 TP2 TP3 TP4 TP5 TP6 TP7 TP8 TP9 TP10 TP11 TP12 TP13 TP14 TP15 TP16 TP17 TP18 TP19 TP20 TP21 TP22 TP23 TP24 TP25 TP26 TP27 TP28 TP29 TP30 TP31 TP32 TP33 TP34 TP35 TP36 TP37 TP38 TP39 TP40

RSVD

NVRAM

NV_CE#0 NV_CE#1 NV_CE#2 NV_CE#3
NV_DQS0 NV_DQS1
NV_DQ0 / NV_IO0 … NV_DQ15 / NV_IO15
NV_ALE NV_CLE
NV_RCOMP
NV_RB#
NV_RE#_WRB0 NV_RE#_WRB1
NV_WE#_CK0 NV_WE#_CK1

PCI

PIRQA# PIRQB# PIRQC# PIRQD#
BT_COMBO_EN# [22]
BOARD_ID6 [9]
BOARD_ID7 [9]
BBS_BIT1 [7]
PCI_GNT3# [7]
MPC_PWR_CTRL#
LCD_BK [21]
PCH_GPIO4
INTH# [26]
REQ1# / GPIO50 (+3V)
REQ2# / GPIO52 (+3V)
REQ3# / GPIO54 (+3V)
GNT1# / GPIO51 (+3V)
GNT2# / GPIO53 (+3V)
GNT3# / GPIO55 (+3V)
PIRQE# / GPIO2 (+3V)
PIRQF# / GPIO3 (+3V)
PIRQG# / GPIO4 (+3V)
PIRQH# / GPIO5 (+3V)

MV EMI add CAP near PCI Clock

TP52 PCI_PME#
PLTRST# [2,14,22,23,25,28,29] R146 100K_4
C406 *33P/50V_4
R287 22_4 CLK_PCI_TPM_R [28] CLK_PCI_TPM
C434 *33P/50V_4
CLK_PCI_CARD_R
R312 22_4 CLK_33M_DEBUG [22]
R286 22_4 CLK_33M_KBC [29]
CLK_PCI_FB
R285 22_4
C404 *33P/50V_4 CLK_PCI_FB_R
C435 *33P/50V_4 CLK_PCI_LPC_R
C405 *33P/50V_4 CLK_PCI_EC_R

CLKOUT_PCI0 CLKOUT_PCI1 CLKOUT_PCI2 CLKOUT_PCI3 CLKOUT_PCI4

USB

USBP0N USBP0P USBP1N USBP1P USBP2N USBP2P USBP3N USBP3P USBP4N USBP4P USBP5N USBP5P USBP6N USBP6P USBP7N USBP7P USBP8N USBP8P USBP9N USBP9P USBP10N USBP10P USBP11N USBP11P USBP12N USBP12P USBP13N USBP13P

USBRBIAS# USB_BIAS R230 22.6/F_4
USBRBIAS

(+3VS5) OC0# / GPIO59 USB_OC0#
(+3VS5) OC1# / GPIO40 USB_OC1#
(+3VS5) OC2# / GPIO41 USB_OC2#
(+3VS5) OC3# / GPIO42 USB_OC3#
(+3VS5) OC4# / GPIO43 USB_OC4#
(+3VS5) OC5# / GPIO9 USB_OC5#
(+3VS5) OC6# / GPIO10 USB_OC6#
(+3VS5) OC7# / GPIO14 USB_OC7#

CougarPoint_Rev_0p7
fcbga989-intel-cougarpoint
AJ0QPRG0T09
IC CTRL(989P)COUGARPOINT QMVY (FCBGA)

WLAN
[22] PCIE_RXN1 / PCIE_RXP1 / PCIE_TXN1 / PCIE_TXP1
C384 0.1U/10V_4 PCIE_TXN1_C
C386 0.1U/10V_4 PCIE_TXP1_C

LAN
[25] PCIE_RXN2_LAN / PCIE_RXP2_LAN / PCIE_TXN2_LAN / PCIE_TXP2_LAN
C374 0.1U/10V_4 PCIE_TXN2_LAN_C
C375 0.1U/10V_4 PCIE_TXP2_LAN_C

Cardreader
[23] PCIE_RXN3_CR / PCIE_RXP3_CR / PCIE_TXN3_CR / PCIE_TXP3_CR
C377 0.1U/10V_4 PCIE_TXN3_CR_C
C380 0.1U/10V_4 PCIE_TXP3_CR_C

U4B

PERN1 PERP1 PETN1 PETP1 PERN2 PERP2 PETN2 PETP2 PERN3 PERP3 PETN3 PETP3 PERN4 PERP4 PETN4 PETP4 PERN5 PERP5 PETN5 PETP5 PERN6 PERP6 PETN6 PETP6 PERN7 PERP7 PETN7 PETP7 PERN8 PERP8 PETN8 PETP8

PCI-E*

SMBUS

(+3VS5) SMBALERT# / GPIO11 E12 SMBALERT#
SMBCLK H14 SMB_PCH_CLK
SMBDATA C9 SMB_PCH_DAT
(+3VS5) SML0ALERT# / GPIO60 A12 DRAMRST_CNTRL_PCH → DRAMRST_CNTRL_PCH [2,12,13]
SML0CLK C8 SMB_ME0_CLK
SML0DATA G12 SMB_ME0_DAT
(+3VS5) SML1ALERT# / PCHHOT# / GPIO74 C13 SML1ALERT# R → TP24
(+3VS5) SML1CLK / GPIO58 E14 SMB_ME1_CLK
(+3VS5) SML1DATA / GPIO75 M16 SMB_ME1_DAT

Controller Link

CL_CLK1 M7 CL_CLK_R → TP49
CL_DATA1 T11 CL_DAT_R → TP26
CL_RST1# P10 CL_RST#_R → TP50

CLOCKS

(+3VS5) PEG_A_CLKRQ# / GPIO47 M10 CLK_PEGA_REQ# R141 *0_4 → VGA_CLK_REQ# [16]
CLKOUT_PEG_A_N AB37 → CLK_PCIE_VGA# [14]
CLKOUT_PEG_A_P AB38 → CLK_PCIE_VGA [14]
GPU
CLKOUT_DMI_N AV22 → CLK_CPU_BCLKN [2]
CLKOUT_DMI_P AU22 → CLK_CPU_BCLKP [2]
CLKOUT_DP_N AM12 → TP19
CLKOUT_DP_P AM13 → TP17
CLKIN_DMI_N BF18 CLK_BUF_PCIE_3GPLL#
CLKIN_DMI_P BE18 CLK_BUF_PCIE_3GPLL
CLKIN_GND1_N BJ30 CLK_BUF_BCLK_N
CLKIN_GND1_P BG30 CLK_BUF_BCLK_P
CLKIN_DOT_96N G24 CLK_BUF_DREFCLK#
CLKIN_DOT_96P E24 CLK_BUF_DREFCLK
CLKIN_SATA_N AK7 CLK_BUF_DREFSSCLK#
CLKIN_SATA_P AK5 CLK_BUF_DREFSSCLK
*27P/50V_4 C424
R277 *1M_4
Y2 *25MHZ
*27P/50V_4 C425
REFCLK14IN K45 CLK_PCH_14M
XTAL25_IN XTAL25_OUT
CLKIN_PCILOOPBACK H45 CLK_PCI_FB
R294 *0_4
R276 0_4
XTAL25_IN V47 XTAL25_IN → PCH_XTAL25_IN [7]
XTAL25_OUT V49 XTAL25_OUT
XCLK_RCOMP Y47 XCLK_RCOMP R334 90.9/F_4 → +1.05V

FLEX CLOCKS

(+3VS5) CLKOUTFLEX0 / GPIO64 K43 CLK_FLEX0 → TP34
(+3VS5) CLKOUTFLEX1 / GPIO65 F47 CLK_FLEX1 → TP35
(+3VS5) CLKOUTFLEX2 / GPIO66 H47 CLK_FLEX2 → TP36
(+3VS5) CLKOUTFLEX3 / GPIO67 K49 CLK_FLEX3 → TP37

CougarPoint_Rev_0p7
fcbga989-intel-cougarpoint
AJ0QPRG0T09
IC CTRL(989P)COUGARPOINT QMVY (FCBGA)

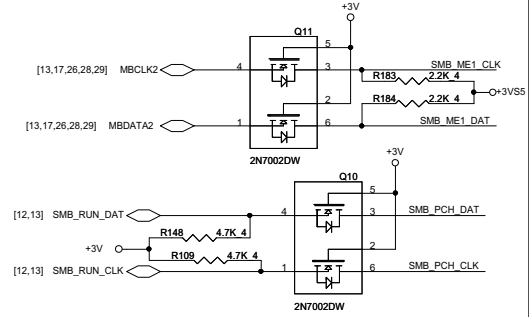
WLAN
[22] CLK_PCIE_WLANN / CLK_PCIE_WLANP → CLKOUT_PCIE0N / CLKOUT_PCIE0P
[22] PCIE_CLKREQ_WLAN# → PCIECLKRQ0# / GPIO73

LAN
[25] CLK_PCIE_LANN / CLK_PCIE_LANP → CLKOUT_PCIE1N / CLKOUT_PCIE1P
[25] PCIE_CLKREQ_LAN# → PCIECLKRQ1# / GPIO18

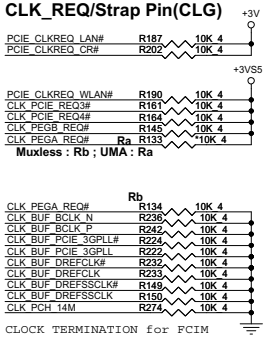
Cardreder
[23] CLK_PCIE_CRN / CLK_PCIE_CRP → CLKOUT_PCIE2N / CLKOUT_PCIE2P
[23] PCIE_CLKREQ_CR# → PCIECLKRQ2# / GPIO20

CLK_PCIE_REQ3# → PCIECLKRQ3# / GPIO25
CLK_PCIE_REQ4# → PCIECLKRQ4# / GPIO26
[9] BOARD_ID0 → PCIECLKRQ5# / GPIO44
CLK_PEGB_REQ# → PEG_B_CLKRQ# / GPIO56
[22] INT_BT_COMBO_EN#
[9] BOARD_ID2
PCIECLKRQ6# / GPIO45
PCIECLKRQ7# / GPIO46
TP23 TP21 CLK_PCH_ITPN CLK_PCH_ITPP → CLKOUT_ITPXDP_N / CLKOUT_ITPXDP_P

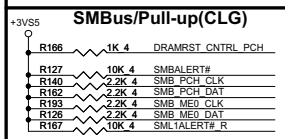
SMBus/Pull-up(CLG)



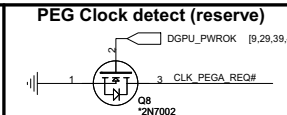
CLK_REQ/Strap Pin(CLG)



SMBus/Pull-up(CLG)



PEG Clock detect (reserve)



Remove for UMA only.

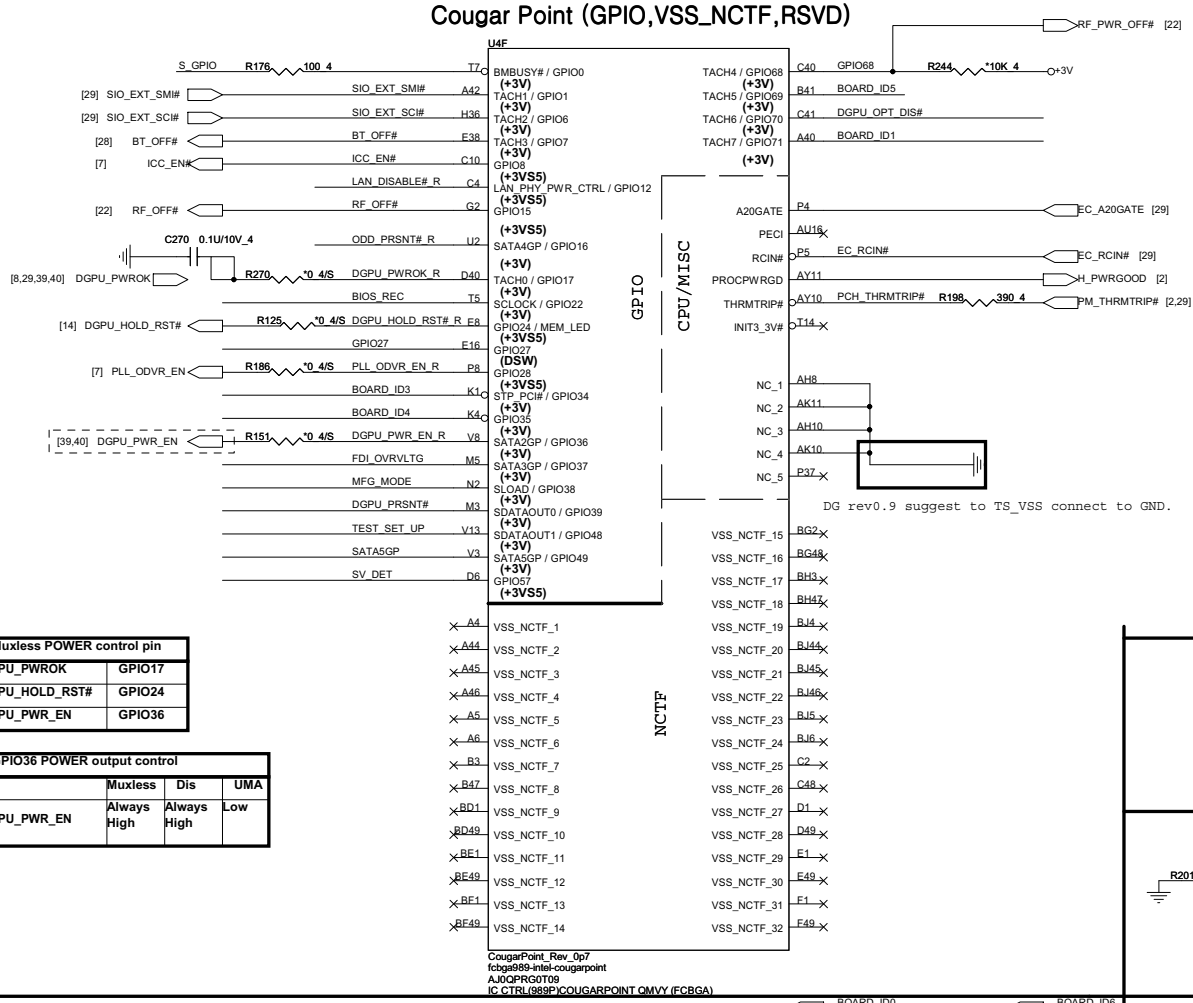
[2,6,7,9,10,12,13,14,16,21,22,23,24,25,26,27,28,29,34,36,38,40] +3V
[6,7,9,10,27,28,29,31,34,35,38,39] +3VS5

NB5

PROJECT : LG3/5 Muxless & UMA
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 3/6 (PCIE/USB/CLK)	2A
Date: Wednesday, March 07, 2012	Sheet 8 of 42	

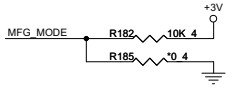
Cougar Point (GPIO,VSS_NCTF,RSVD)



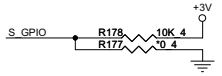
Muxless POWER control pin	
DGPU_PWROK	GPIO17
DGPU_HOLD_RST#	GPIO24
DGPU_PWR_EN	GPIO36

GPIO36 POWER output control			
	Muxless	Dis	UMA
DGPU_PWR_EN	Always High	Always High	Low

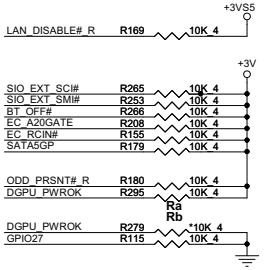
MFG-TEST



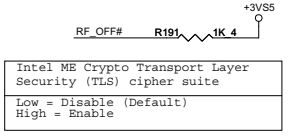
SGPIO

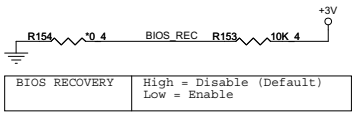


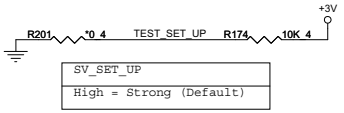
GPIO Pull-up/Pull-down(CLG)

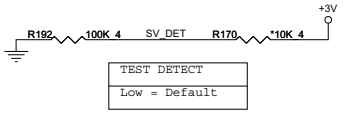


	Select
VGA	Ra
UMA	Rb

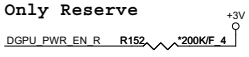








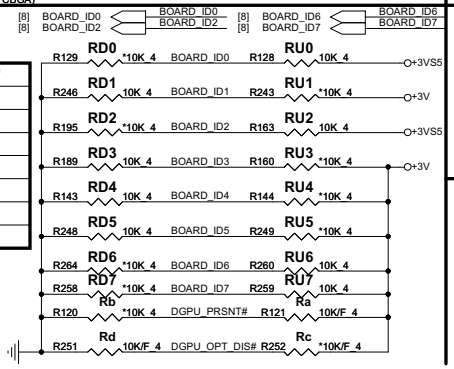
Only Reserve



Chief River BOARD ID SETTING

BOARD_ID0	GPIO44	MODEL BIT0
BOARD_ID1	GPIO71	MODEL BIT1
BOARD_ID2	GPIO46	MODEL BIT2
BOARD_ID3	GPIO34	MODEL BIT3
BOARD_ID4	GPIO35	Reserve and pull low
BOARD_ID5	GPIO69	Reserve and pull low
DGPU_PRSNT#	GPIO39	VGA =1 , UMA=0
DGPU_OPT_DIS#	GPIO70	Muxless=0, Dis only=1

Board ID [3:0]	Model Name
0100	LG3
0101	LG5



[2,6,7,8,10,12,13,14,16,21,22,23,24,25,26,27,28,29,34,36,38,40] +3V
[6,7,8,10,27,28,29,31,34,35,38,39] +3VS5

PROJECT : LG3/5 Muxless & UMA
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 4/6 (GPIO/MISC)	2A
NB5	Date: Wednesday, March 07, 2012	Sheet 9 of 42

Cougar Point-M (POWER)

COUGAR POINT (POWER)

10

U4J

Clock and Miscellaneous | USB | PCI/GPIO/LPC | SATA | MISC | CPU | RTC | HDA

U4G

VCC CORE | CRT | LVDS | HVCMOS | VCCIO | DMI | FDI | NAND / SPI

Near PCH

1.01A (60mils)

3mA (10mils)

1.3 A (60mils)

2.925 A (140mils)

119mA (20mils)

119mA (15mils)

266mA (20mils)

1.01A (60mils)

160mA (20mils)

65mA (10mils)

8mA (10mils)

55mA (10mils)

95mA (10mils)

160mA (15mils)

(Mobile 1.5V)

VCC5REFSUS=1mA

V5REF= 1mA

V_PROC_IO=1mA (10mils)

VCCRTC<1mA (10mils)

10mA (10mils)

20mA (10mils)

1mA (10mils)

60mA (10mils)

Muxless : Ra
UMA : Ra
DIS : Rb

42mA (10mils)

190 mA (15mils)

20mA (10mils)

65mA (10mils)

8mA (10mils)

UMA & Muxless Only, If have power noise issue then stuff it.

CougarPoint_Rev_0p7
fcbga989-intel-cougarpoint
AJ0QPRG0T09
IC CTRL(989P)COUGARPOINT QMVY (FCBGA)

G9191-330T1U
U7

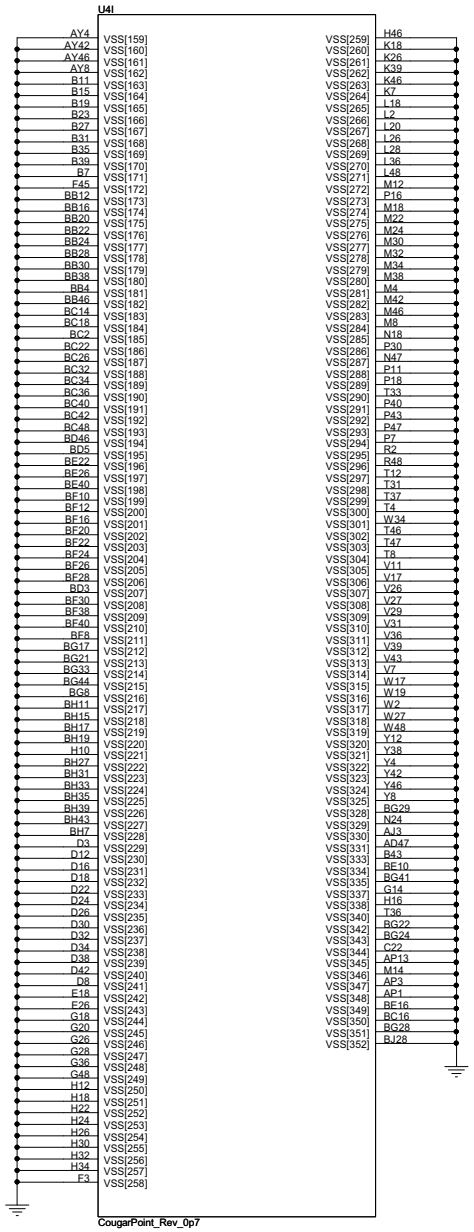
[2,4,22] +1.5V_CPU
[4,7,35] +1.8V
[2,4,12,13,27,32,39] +1.05VSUS
+1.05V_VTT
[2,4,6,7,8,29,34,36] +1.05V
[7,21,22,23,24,26,28,38] +5V
[26,27,31,32,33,34,35,36,37,38,39,40] +5VS5
[6,7,8,9,27,28,29,31,34,35,38,39] +3VS5
[6,7,29] +3V_RTC
[2,6,7,8,9,12,13,14,16,21,22,23,24,25,26,27,28,29,34,36,38,40] +3V

NB5

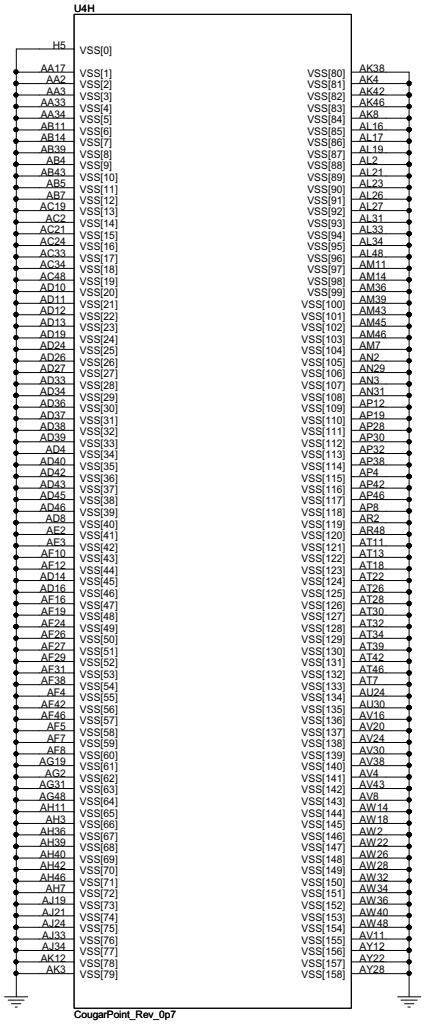
PROJECT : LG3/5 Muxless & UMA
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 5/6 (POWER)	2A
Date: Wednesday, March 07, 2012	Sheet 10 of 42	

IBEX PEAK-M (GND)

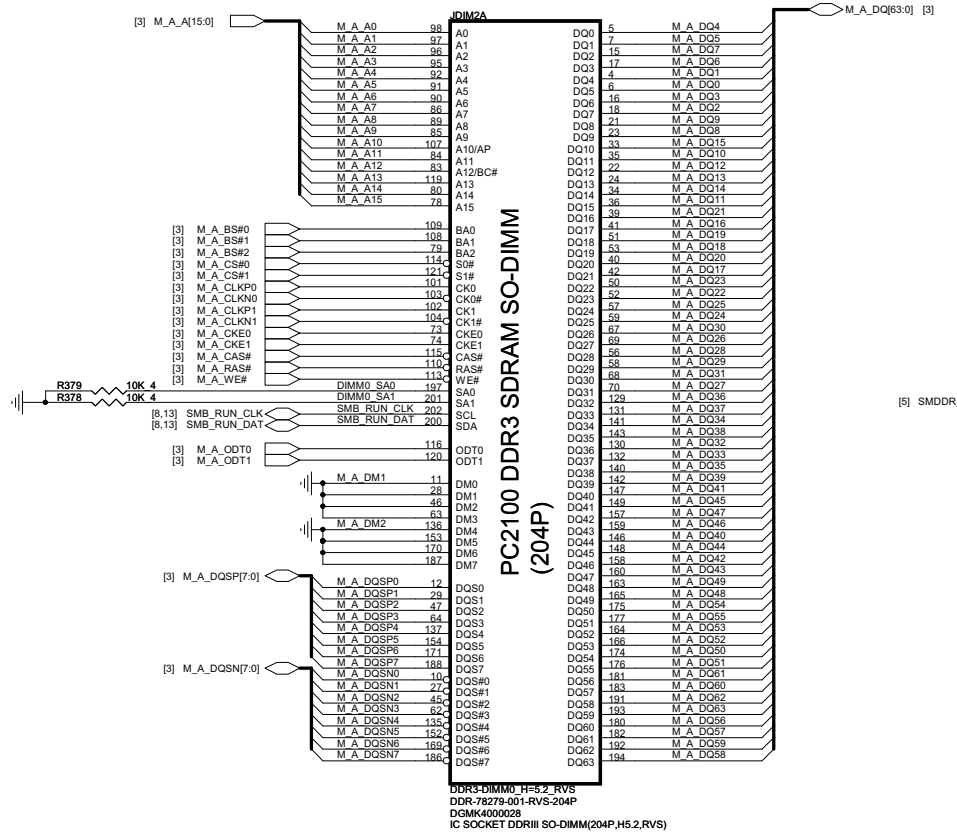


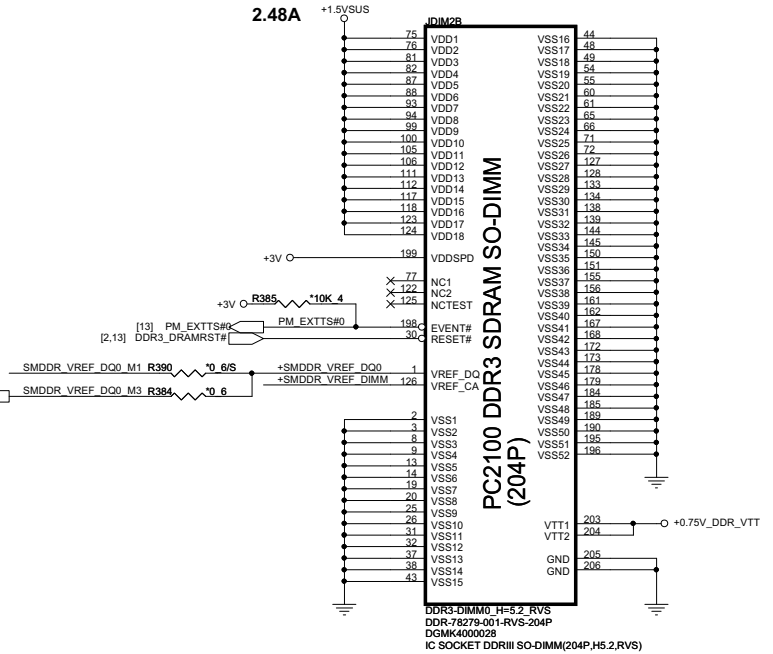
IBEX PEAK-M (GND)



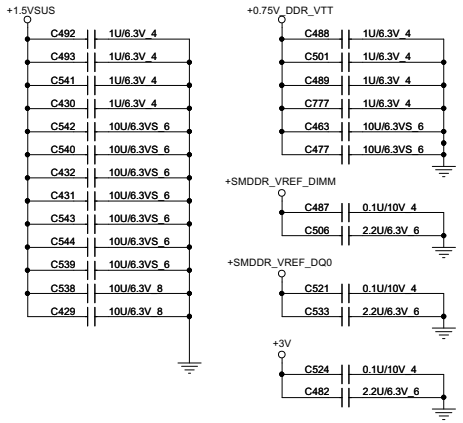
PROJECT : LG3/5 Muxless & UMA
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 6/6 (GND)	2A
NB5	Date: Wednesday, March 07, 2012	Sheet 11 of 42

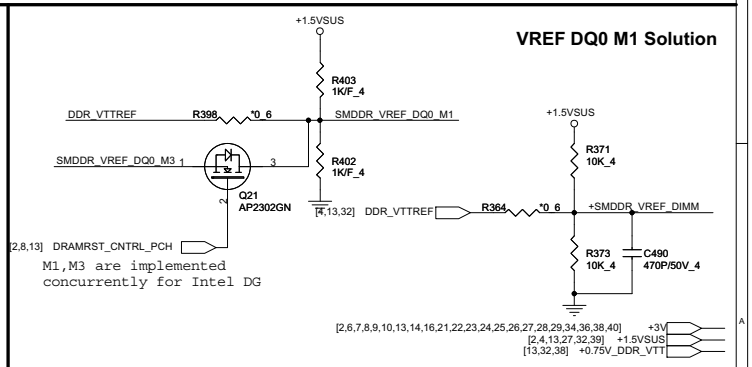




Place these Caps near So-Dimm0.

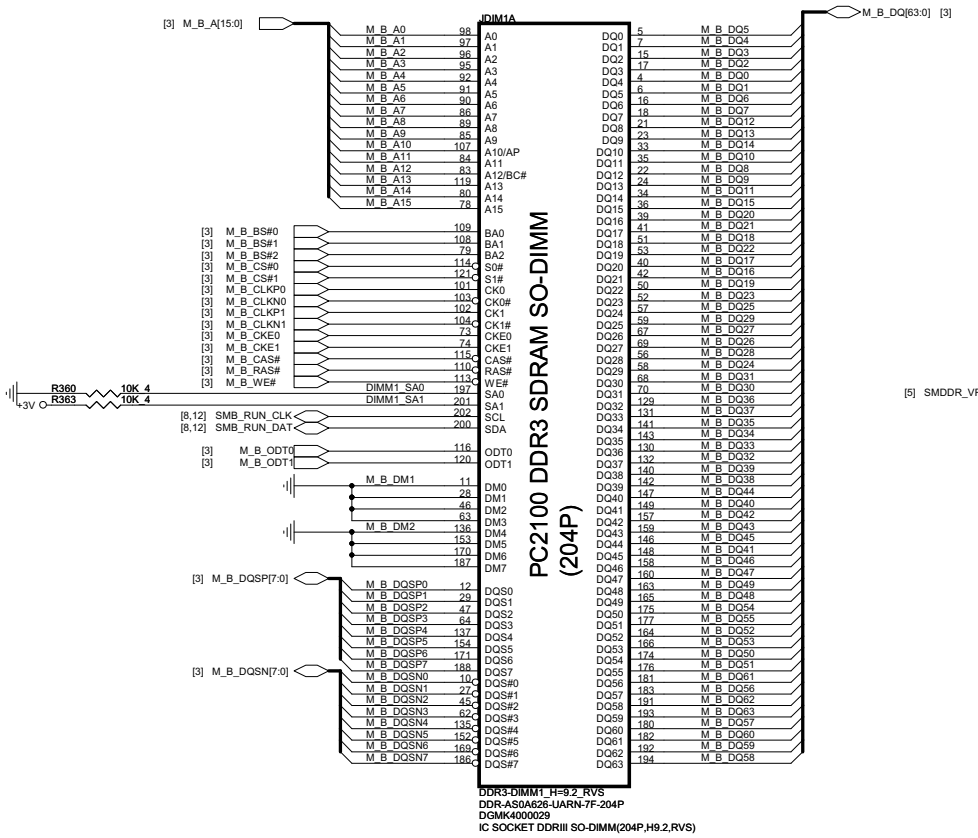


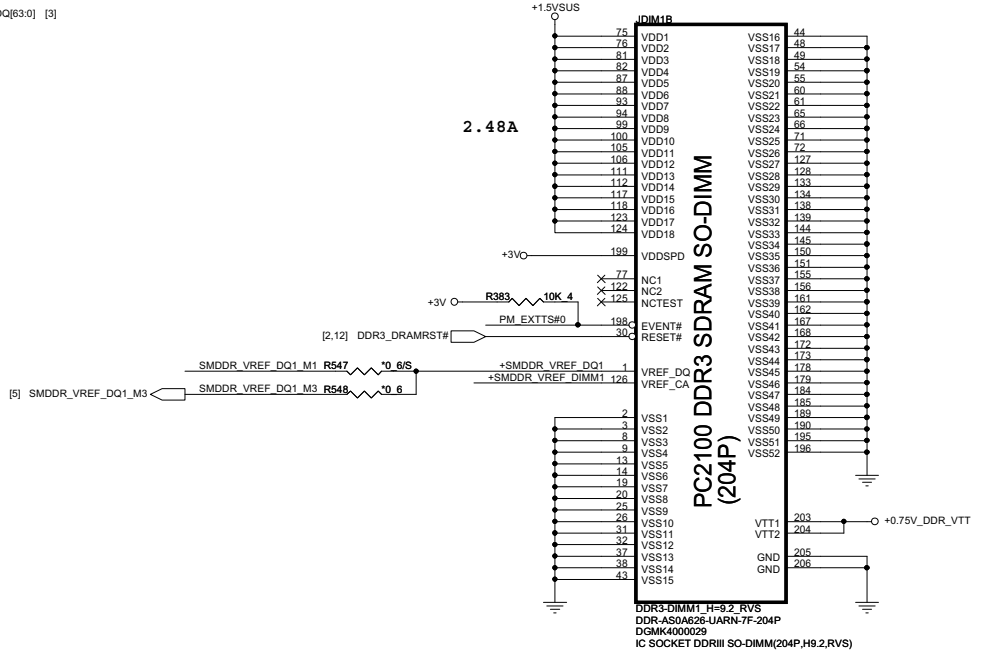
VREF DQ0 M1 Solution

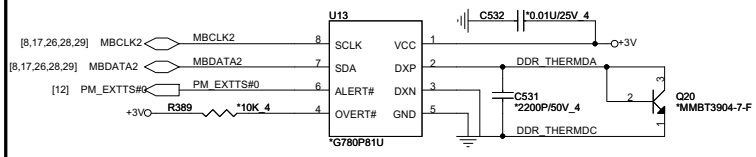


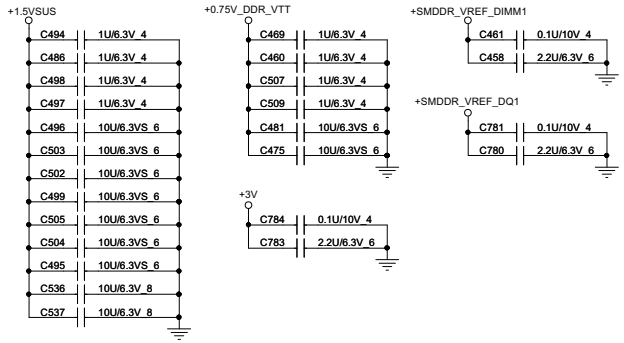
PROJECT : LG3/5 Muxless & UMA
Quanta Computer Inc.

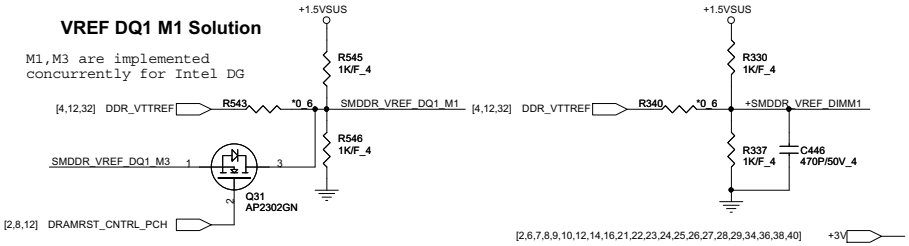
Size	Document Number	Rev
Custom	DDR3 DIMM0-RVS (5.2H)	2A
NB5	Date: Wednesday, March 07, 2012	Sheet 12 of 42



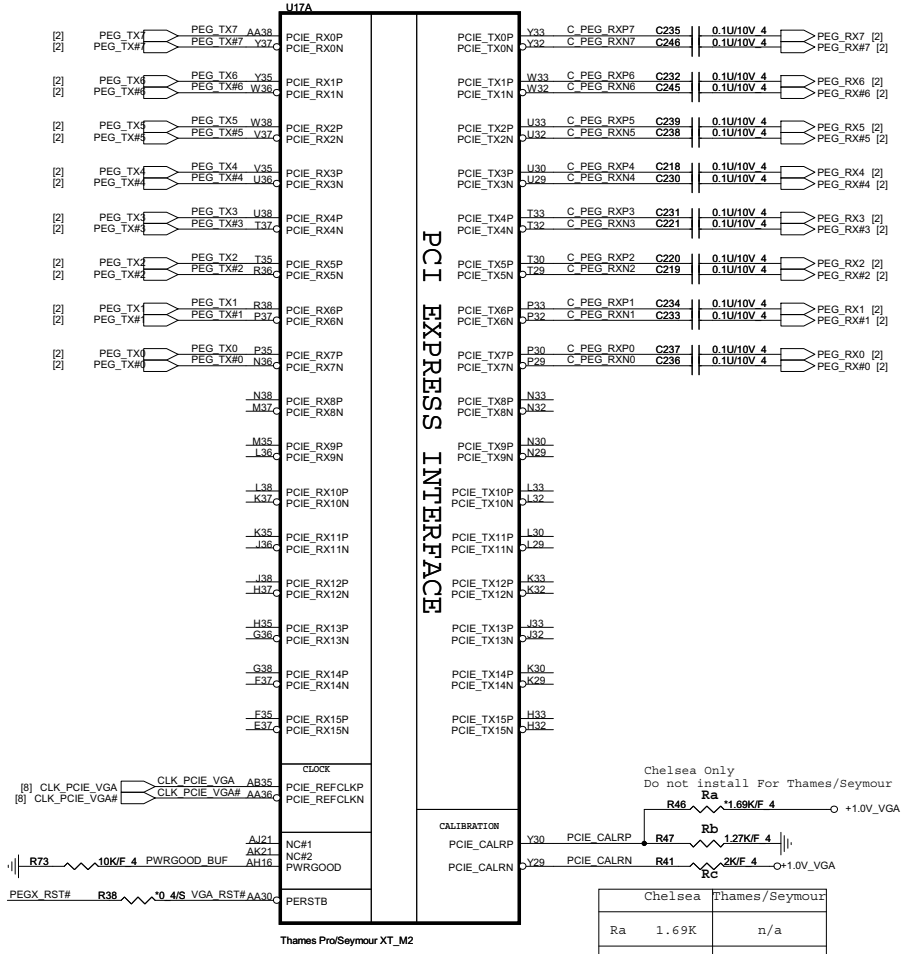








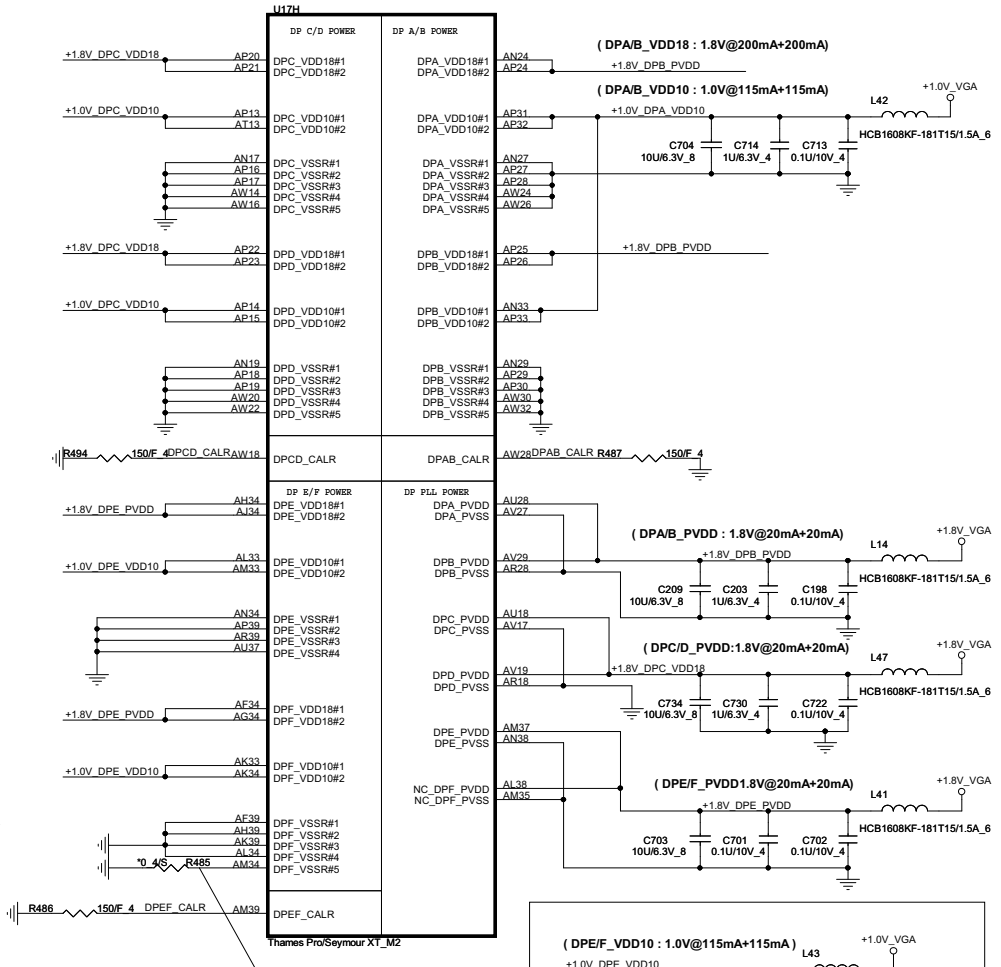
PROJECT :	LG3/5 Muxless & UMA
Quanta Computer Inc.	
NB5	Size: Custom; Document Number: DDR3 DIMM1-RVS (9.2H); Rev: 2A
Date: Wednesday, March 07, 2012	Sheet 13 of 42



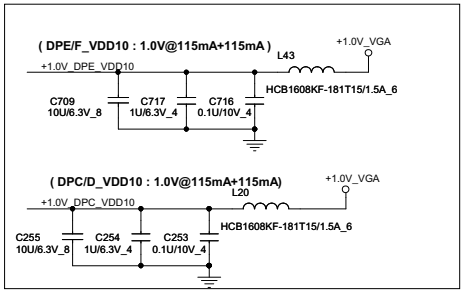
Chelsea Only
Do not install For Thames/Seymour

R46 Ra *1.69K/F_4 +1.0V_VGA
R47 Rb 1.27K/F_4
R41 Rc 2K/F_4 +1.0V_VGA

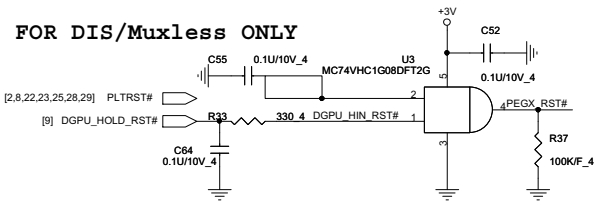
	Chelsea	Thames/Seymour
Ra	1.69K	n/a
Rb	n/a	1.27K
Rc	1K	2K



Thames INSTALL, do not install for Chelsea
PS_0 should be tied to GND on Thames



FOR DIS/Muxless ONLY



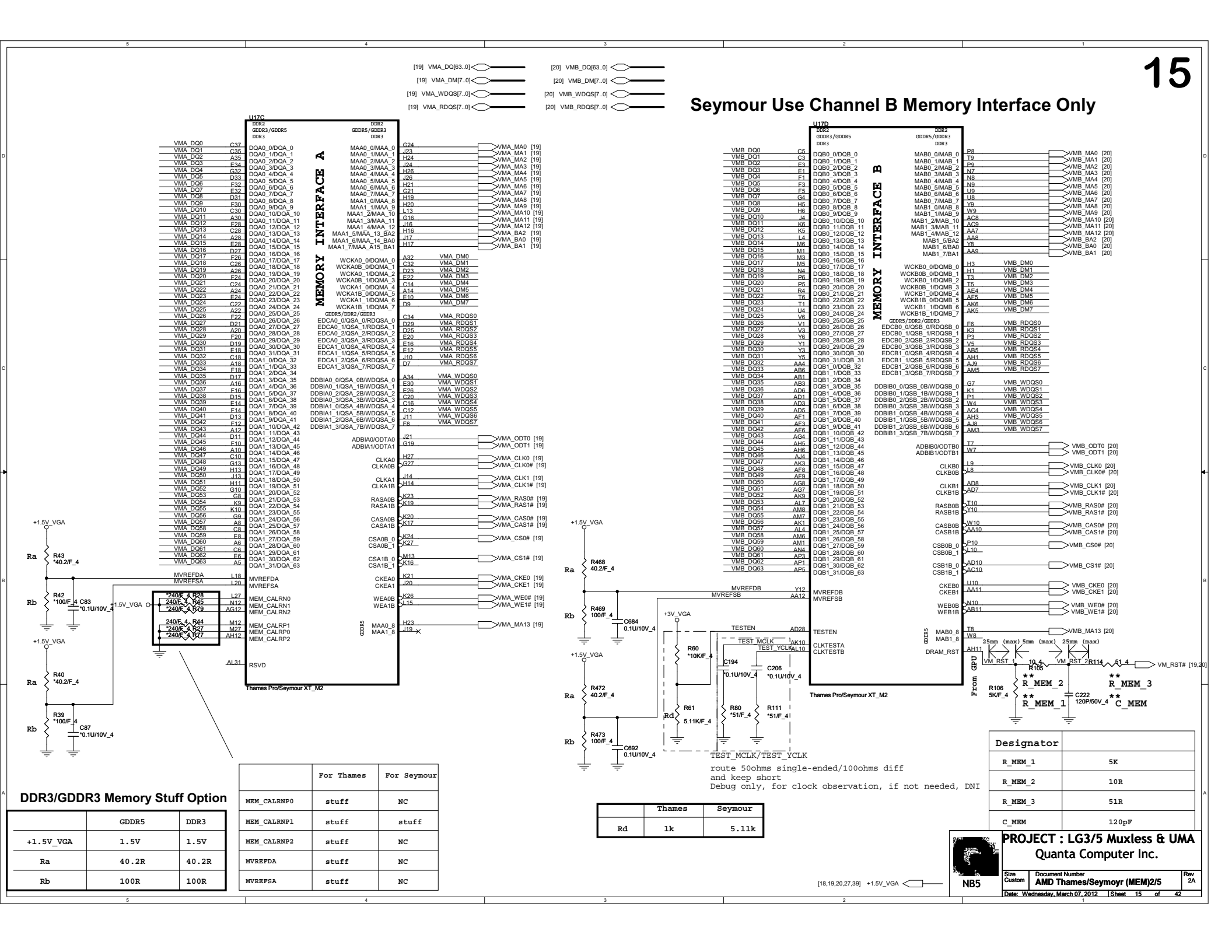
[2,6,7,8,9,10,12,13,16,21,22,23,24,25,26,27,28,29,34,36,38,40] +3V
[16,18,39] +1.8V_VGA
[16,18,39] +1.0V_VGA

NB5	PROJECT : LG3/5 Muxless & UMA Quanta Computer Inc.
Size: Custom	Document Number: AMD Thames/Seymoyr (MEM)1/5
Rev: 2A	
Date: Wednesday, March 07, 2012	Sheet 14 of 42

Seymour Use Channel B Memory Interface Only

[19] VMA_DQ[63..0] [19] VMA_DM[7..0] [19] VMA_WDQS[7..0] [19] VMA_RDQS[7..0]

[20] VMB_DQ[63..0] [20] VMB_DM[7..0] [20] VMB_WDQS[7..0] [20] VMB_RDQS[7..0]



route 50ohms single-ended/100ohms diff
and keep short
Debug only, for clock observation, if not needed, DNI

TEST_MCLK/TEST_YCLK

[18,19,20,27,39] +1.5V_VGA

DDR3/GDDR3 Memory Stuff Option

	GDDR5	DDR3
+1.5V_VGA	1.5V	1.5V
Ra	40.2R	40.2R
Rb	100R	100R

	For Thames	For Seymour
MEM_CALRNP0	stuff	NC
MEM_CALRNP1	stuff	stuff
MEM_CALRNP2	stuff	NC
MVREFDA	stuff	NC
MVREFSA	stuff	NC

	Thames	Seymour
Rd	1k	5.11k

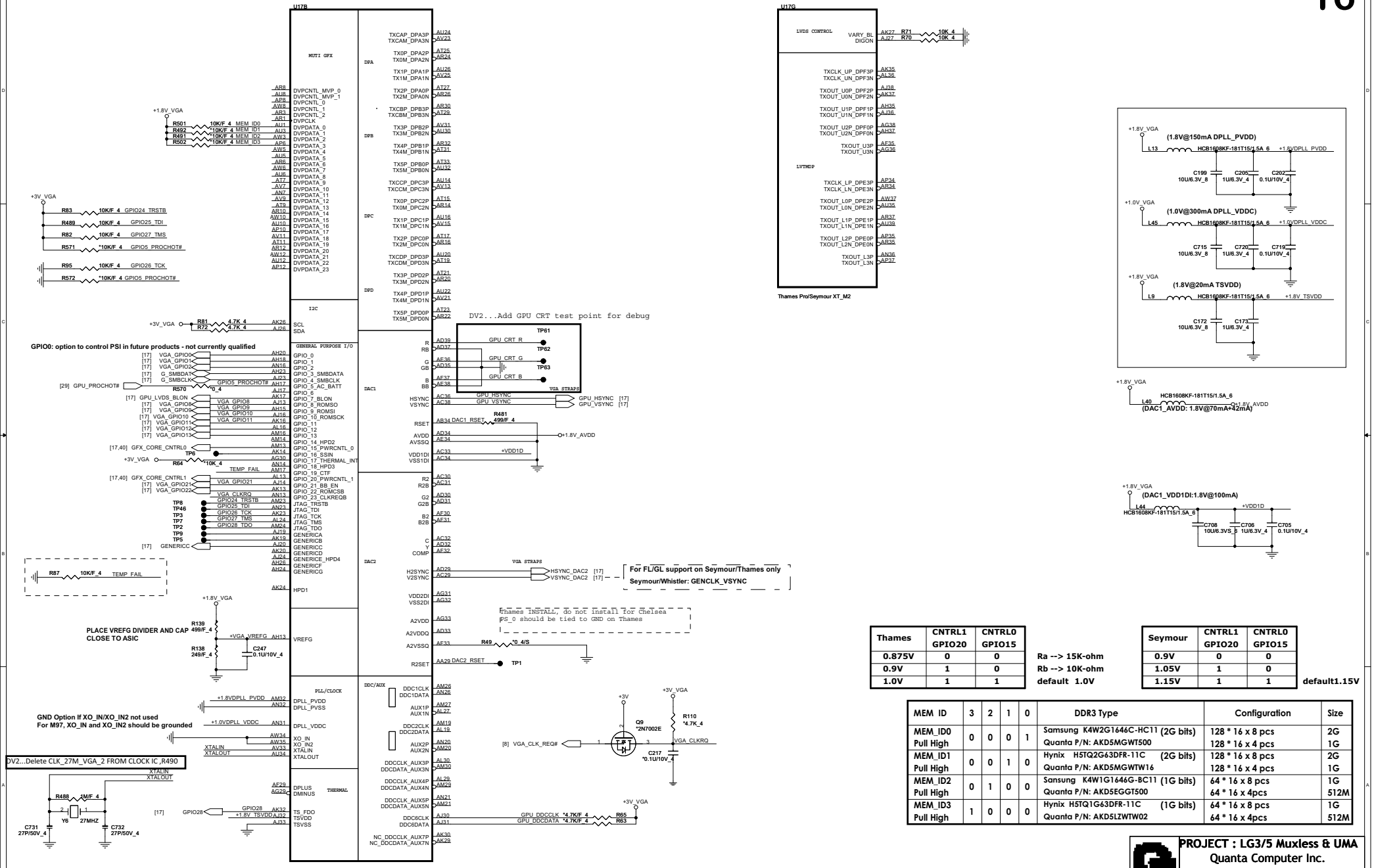
Designator	
R_MEM_1	5K
R_MEM_2	10R
R_MEM_3	51R
C_MEM	120pF

NB5

PROJECT : LG3/5 Muxless & UMA
Quanta Computer Inc.

Size	Document Number	Rev
Custom	AMD Thames/Seymoyr (MEM)2/5	2A

Date: Wednesday, March 07, 2012 Sheet 15 of 42



Thames	CNTRL1 GPIO20	CNTRL0 GPIO15
0.875V	0	0
0.9V	1	0
1.0V	1	1

Ra --> 15K-ohm
Rb --> 10K-ohm
default 1.0V

Seymour	CNTRL1 GPIO20	CNTRL0 GPIO15
0.9V	0	0
1.05V	1	0
1.15V	1	1

default1.15V

MEM_ID	3	2	1	0	DDR3 Type	Configuration	Size
MEM_ID0 Pull High	0	0	0	1	Samsung K4W2G1646C-HC11 (2G bits)	128 * 16 x 8 pcs	2G
					Quanta P/N: AKD5MGWT500	128 * 16 x 4 pcs	1G
MEM_ID1 Pull High	0	0	1	0	Hynix H5TQ2G63DFR-11C (2G bits)	128 * 16 x 8 pcs	2G
					Quanta P/N: AKD5MGWTW16	128 * 16 x 4 pcs	1G
MEM_ID2 Pull High	0	1	0	0	Sansung K4W1G1646G-BC11 (1G bits)	64 * 16 x 8 pcs	1G
					Quanta P/N: AKD5EGGT500	64 * 16 x 4pcs	512M
MEM_ID3 Pull High	1	0	0	0	Hynix H5TQ1G63DFR-11C (1G bits)	64 * 16 x 8 pcs	1G
					Quanta P/N: AKD5LZWTW02	64 * 16 x 4pcs	512M

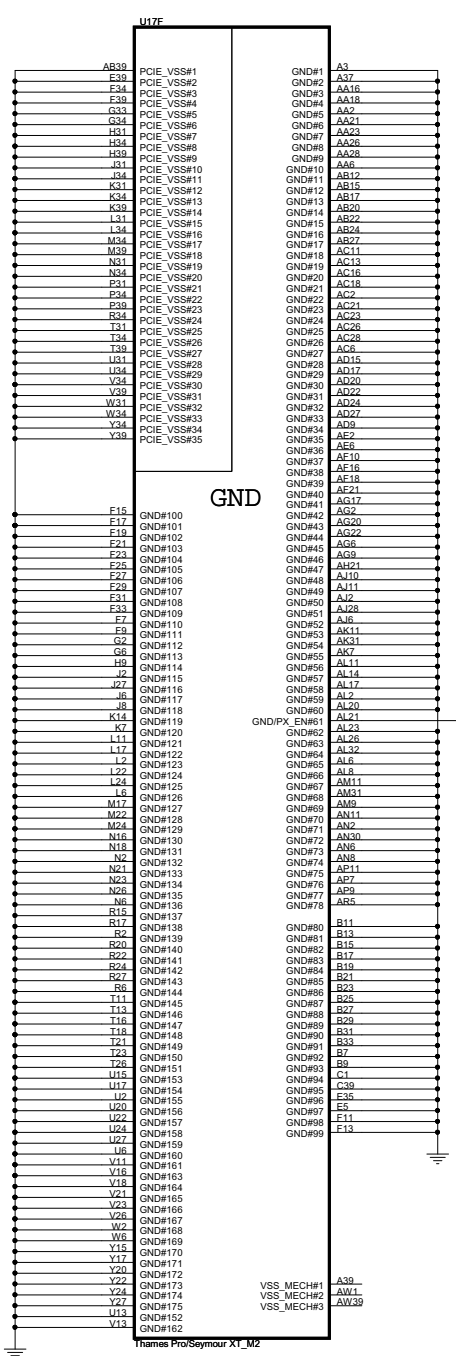
[14,18,39] +1.0V_VGA
[14,18,39] +1.8V_VGA
[15,17,18,39,40] +3V_VGA

NB5

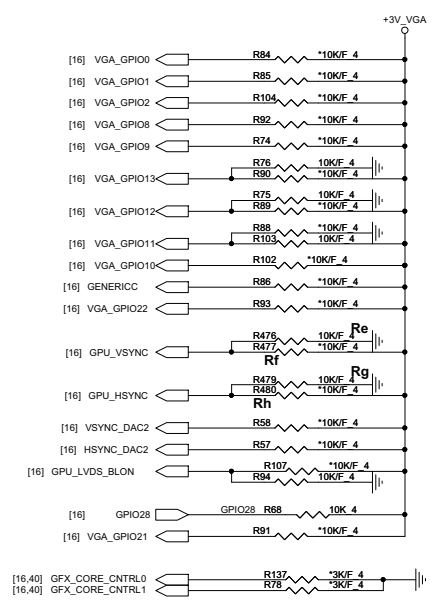
PROJECT : LG3/5 Muxless & UMA
Quanta Computer Inc.

Size	Document Number	Rev
Custom	AMD Thames/Seymoyr DISPLAY3/5	2A

Date: Wednesday, March 07, 2012 | Sheet 16 of 42

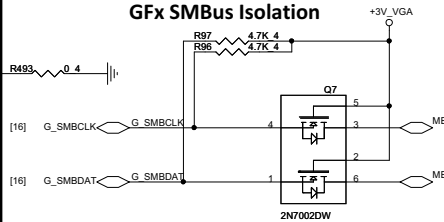


STRAPS

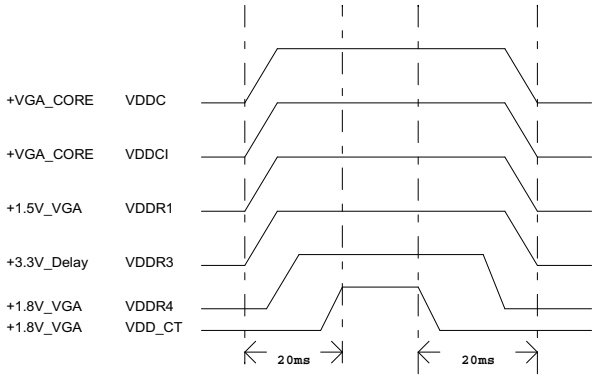


CONFIGURATION STRAPS -- SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET				
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	X
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIE Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIE Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1
BIF_VGA DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	XXX
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	X
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled	X
			NOTE: ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOS ARE USEED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET	
RESERVED RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA NA	GENLK_CLK GPIO8 GPIO21 GENERICC	Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only)	0 0 0 0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

GFx SMBus Isolation



Power Up/Down Sequence



GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

Memory Aperture size

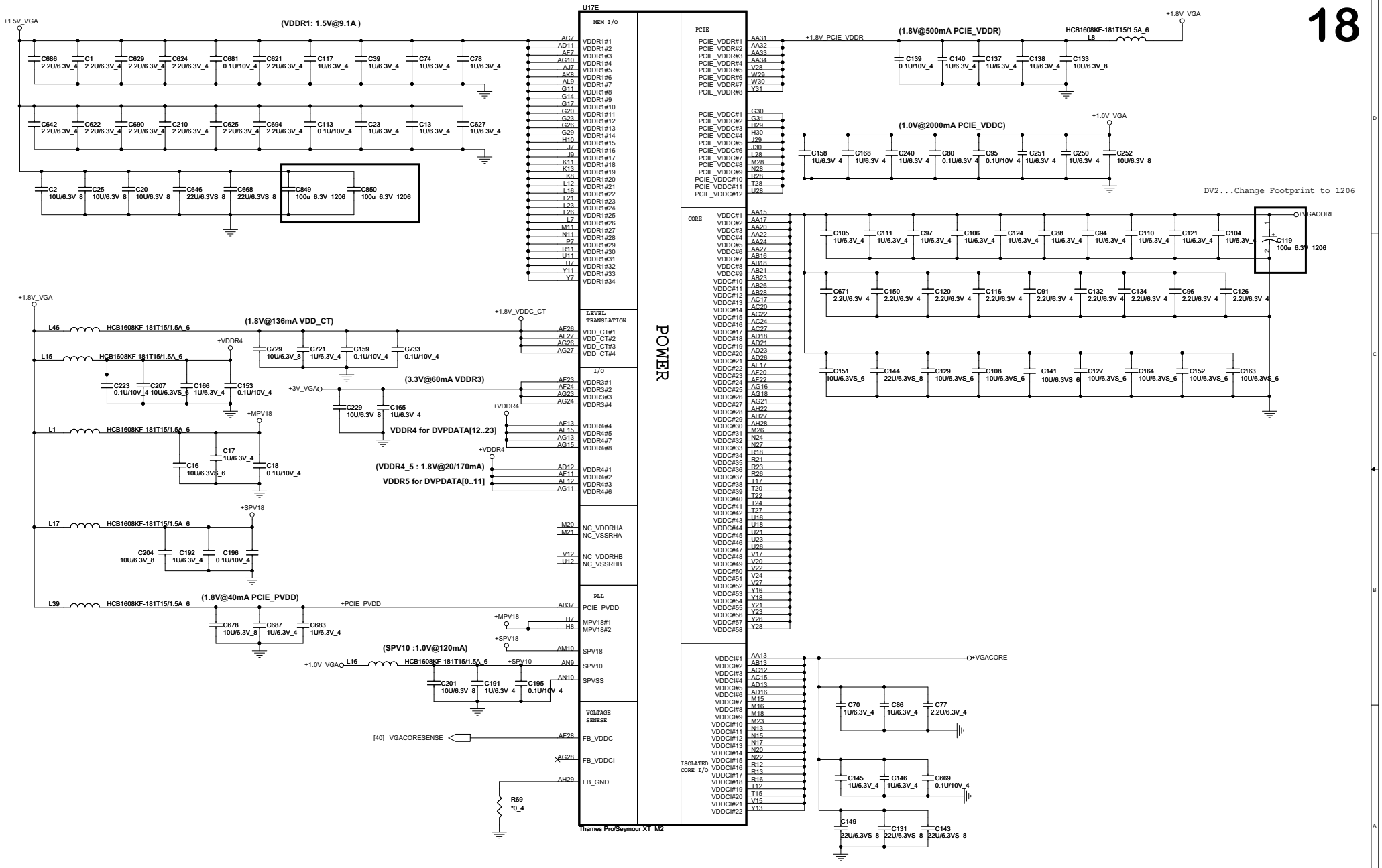
[15,16,18,39,40] +3V_VGA

NB5

PROJECT : LG3/5 Muxless & UMA
Quanta Computer Inc.

Size	Document Number	Rev
Custom	AMD Thames/Seymoyr(GD&Str)4/5	2A

Date: Wednesday, March 07, 2012 Sheet 17 of 42



[2,6,7,8,9,10,12,13,14,16,21,22,23,24,25,26,27,28,29,34,36,38,40] +3V
[7,10,21,22,23,24,26,28,38] +5V
[14,16,39] +1.0V_VGA
[40] +VGACORE
[15,19,20,27,39] +1.5V_VGA
[14,16,39] +1.8V_VGA
[15,16,17,39,40] +3V_VGA

NB5

PROJECT : LG3/5 Muxless & UMA
Quanta Computer Inc.

Size	Document Number	Rev
Custom	AMD Thames/Seymoyr(POWER) 5/5	2A
Date: Wednesday, March 07, 2012	Sheet 18 of 42	

CHANNEL A: 256MB/512MB DDR3

[15] VMA_DQ[63..0]
[15] VMA_DM[7..0]
[15] VMA_WDQS[7..0]
[15] VMA_RDQS[7..0]

VRAM1 — 100-BALL SDRAM DDR3 *K4W1G1646E-HC12

VREFC_VMA1 M9 VREFCA
VREFD_VMA1 H2 VREFDQ

[15] VMA_MA0 N4 A0
[15] VMA_MA1 P8 A1
[15] VMA_MA2 P4 A2
[15] VMA_MA3 N3 A3
[15] VMA_MA4 P9 A4
[15] VMA_MA5 P3 A5
[15] VMA_MA6 R9 A6
[15] VMA_MA7 R3 A7
[15] VMA_MA8 T9 A8
[15] VMA_MA9 R4 A9
[15] VMA_MA10 L8 A10/AP
[15] VMA_MA11 R8 A11
[15] VMA_MA12 N8 A12/BC
[15] VMA_MA13 T4 A13
T8 A14
M8 A15/BA3

[15] VMA_BA0 M3 BA0
[15] VMA_BA1 N9 BA1
[15] VMA_BA2 M4 BA2

[15] VMA_CLK0 J8 CK
[15] VMA_CLK0# K8 CK
[15] VMA_CKE0 K10 CKE/CKE0

[15] VMA_ODT0 K2 ODT/ODT0
[15] VMA_CS0# L3 CS /CS0
[15] VMA_RAS0# J4 RAS
[15] VMA_CAS0# K4 CAS
[15] VMA_WE0# L4 WE

VMA_RDQS0 F4 DQSL
VMA_RDQS2 C8 DQSU

VMA_DM0 E8 DML
VMA_DM2 D4 DMU

VMA_WDQS0 G4 DQSL
VMA_WDQS2 B8 DQSU

[15,20] VM_RST# T3 RESET

VMA_ZQ1 L9 ZQ/ZQ0

DQL0 F4 VMA_DQ0
DQL1 F8 VMA_DQ7
DQL2 F3 VMA_DQ2
DQL3 F9 VMA_DQ6
DQL4 H4 VMA_DQ3
DQL5 H9 VMA_DQ4
DQL6 G3 VMA_DQ1
DQL7 H8 VMA_DQ5

D8 VMA_DQ17
C4 VMA_DQ22
C9 VMA_DQ23
C3 VMA_DQ18
A8 VMA_DQ21
A3 VMA_DQ19
B9 VMA_DQ20
A4 VMA_DQ16

+1.5V_VGA

VDD#B3 B3
VDD#D10 D10
VDD#G8 G8
VDD#K3 K3
VDD#K9 K9
VDD#N2 N2
VDD#N10 N10
VDD#R2 R2
VDD#R10 R10

+1.5V_VGA

VDDQ#A2 A2
VDDQ#A9 A9
VDDQ#C2 C2
VDDQ#C10 C10
VDDQ#D3 D3
VDDQ#E10 E10
VDDQ#F2 F2
VDDQ#H3 H3
VDDQ#H10 H10

VSS#A10 A10
VSS#B4 B4
VSS#E2 E2
VSS#G9 G9
VSS#J3 J3
VSS#J9 J9
VSS#M2 M2
VSS#M10 M10
VSS#P2 P2
VSS#P10 P10
VSS#T2 T2
VSS#T10 T10

VSSQ#B2 B2
VSSQ#B10 B10
VSSQ#D2 D9
VSSQ#D9 E3
VSS#E3 E9
VSSQ#E9 F10
VSSQ#F10 G2
VSSQ#G2 G10
VSSQ#G10

NC A1
NC T1
NC A11
NC T11
NC/ODT1 J2
NC/CS1 L2
NC/CE1 J10
NC/ZQ1 L10

Should be 240 Ohms +-1%

R2 *243/F_4

VRAM5 — 100-BALL SDRAM DDR3 *K4W1G1646E-HC12

VREFC_VMA2 M9 VREFCA
VREFD_VMA2 H2 VREFDQ

VMA_MA0 N4 A0
VMA_MA1 P8 A1
VMA_MA2 P4 A2
VMA_MA3 N3 A3
VMA_MA4 P9 A4
VMA_MA5 P3 A5
VMA_MA6 R9 A6
VMA_MA7 R3 A7
VMA_MA8 T9 A8
VMA_MA9 R4 A9
VMA_MA10 L8 A10/AP
VMA_MA11 R8 A11
VMA_MA12 N8 A12/BC
VMA_MA13 T4 A13
T8 A14
M8 A15/BA3

VMA_BA0 M3 BA0
VMA_BA1 N9 BA1
VMA_BA2 M4 BA2

VMA_CLK0 J8 CK
VMA_CLK0# K8 CK
VMA_CKE0 K10 CKE/CKE0

VMA_ODT0 K2 ODT/ODT0
VMA_CS0# L3 CS /CS0
VMA_RAS0# J4 RAS
VMA_CAS0# K4 CAS
VMA_WE0# L4 WE

VMA_RDQS1 F4 DQSL
VMA_RDQS3 C8 DQSU

VMA_DM1 E8 DML
VMA_DM3 D4 DMU

VMA_WDQS1 G4 DQSL
VMA_WDQS3 B8 DQSU

VM_RST# T3 RESET

VMA_ZQ2 L9 ZQ/ZQ0

DQL0 F4 VMA_DQ13
DQL1 F8 VMA_DQ12
DQL2 F3 VMA_DQ15
DQL3 F9 VMA_DQ10
DQL4 H4 VMA_DQ11
DQL5 H9 VMA_DQ8
DQL6 G3 VMA_DQ14
DQL7 H8 VMA_DQ9

D8 VMA_DQ31
C4 VMA_DQ25
C9 VMA_DQ30
C3 VMA_DQ26
A8 VMA_DQ29
A3 VMA_DQ27
B9 VMA_DQ28
A4 VMA_DQ24

+1.5V_VGA

VDD#B3 B3
VDD#D10 D10
VDD#G8 G8
VDD#K3 K3
VDD#K9 K9
VDD#N2 N2
VDD#N10 N10
VDD#R2 R2
VDD#R10 R10

+1.5V_VGA

VDDQ#A2 A2
VDDQ#A9 A9
VDDQ#C2 C2
VDDQ#C10 C10
VDDQ#D3 D3
VDDQ#E10 E10
VDDQ#F2 F2
VDDQ#H3 H3
VDDQ#H10 H10

VSS#A10 A10
VSS#B4 B4
VSS#E2 E2
VSS#G9 G9
VSS#J3 J3
VSS#J9 J9
VSS#M2 M2
VSS#M10 M10
VSS#P2 P2
VSS#P10 P10
VSS#T2 T2
VSS#T10 T10

VSSQ#B2 B2
VSSQ#B10 B10
VSSQ#D2 D9
VSSQ#D9 E3
VSS#E3 E9
VSSQ#E9 F10
VSSQ#F10 G2
VSSQ#G2 G10
VSSQ#G10

NC A1
NC T1
NC A11
NC T11
NC/ODT1 J2
NC/CS1 L2
NC/CE1 J10
NC/ZQ1 L10

Should be 240 Ohms +-1%

R451 *243/F_4

VRAM2 — 100-BALL SDRAM DDR3 *K4W1G1646E-HC12

VREFC_VMA3 M9 VREFCA
VREFD_VMA3 H2 VREFDQ

VMA_MA0 N4 A0
VMA_MA1 P8 A1
VMA_MA2 P4 A2
VMA_MA3 N3 A3
VMA_MA4 P9 A4
VMA_MA5 P3 A5
VMA_MA6 R9 A6
VMA_MA7 R3 A7
VMA_MA8 T9 A8
VMA_MA9 R4 A9
VMA_MA10 L8 A10/AP
VMA_MA11 R8 A11
VMA_MA12 N8 A12/BC
VMA_MA13 T4 A13
T8 A14
M8 A15/BA3

VMA_BA0 M3 BA0
VMA_BA1 N9 BA1
VMA_BA2 M4 BA2

[15] VMA_CLK1 J8 CK
[15] VMA_CLK1# K8 CK
[15] VMA_CKE1 K10 CKE/CKE0

[15] VMA_ODT1 K2 ODT/ODT0
[15] VMA_CS1# L3 CS /CS0
[15] VMA_RAS1# J4 RAS
[15] VMA_CAS1# K4 CAS
[15] VMA_WE1# L4 WE

VMA_RDQS5 F4 DQSL
VMA_RDQS4 C8 DQSU

VMA_DM5 E8 DML
VMA_DM4 D4 DMU

VMA_WDQS5 G4 DQSL
VMA_WDQS4 B8 DQSU

VM_RST# T3 RESET

VMA_ZQ3 L9 ZQ/ZQ0

DQL0 F4 VMA_DQ46
DQL1 F8 VMA_DQ44
DQL2 F3 VMA_DQ47
DQL3 F9 VMA_DQ43
DQL4 H4 VMA_DQ45
DQL5 H9 VMA_DQ41
DQL6 G3 VMA_DQ40
DQL7 H8 VMA_DQ42

D8 VMA_DQ34
C4 VMA_DQ36
C9 VMA_DQ35
C3 VMA_DQ37
A8 VMA_DQ32
A3 VMA_DQ39
B9 VMA_DQ33
A4 VMA_DQ38

+1.5V_VGA

VDD#B3 B3
VDD#D10 D10
VDD#G8 G8
VDD#K3 K3
VDD#K9 K9
VDD#N2 N2
VDD#N10 N10
VDD#R2 R2
VDD#R10 R10

+1.5V_VGA

VDDQ#A2 A2
VDDQ#A9 A9
VDDQ#C2 C2
VDDQ#C10 C10
VDDQ#D3 D3
VDDQ#E10 E10
VDDQ#F2 F2
VDDQ#H3 H3
VDDQ#H10 H10

VSS#A10 A10
VSS#B4 B4
VSS#E2 E2
VSS#G9 G9
VSS#J3 J3
VSS#J9 J9
VSS#M2 M2
VSS#M10 M10
VSS#P2 P2
VSS#P10 P10
VSS#T2 T2
VSS#T10 T10

VSSQ#B2 B2
VSSQ#B10 B10
VSSQ#D2 D9
VSSQ#D9 E3
VSS#E3 E9
VSSQ#E9 F10
VSSQ#F10 G2
VSSQ#G2 G10
VSSQ#G10

NC A1
NC T1
NC A11
NC T11
NC/ODT1 J2
NC/CS1 L2
NC/CE1 J10
NC/ZQ1 L10

Should be 240 Ohms +-1%

R450 *243/F_4

VRAM6 — 100-BALL SDRAM DDR3 *K4W1G1646E-HC12

VREFC_VMA4 M9 VREFCA
VREFD_VMA4 H2 VREFDQ

VMA_MA0 N4 A0
VMA_MA1 P8 A1
VMA_MA2 P4 A2
VMA_MA3 N3 A3
VMA_MA4 P9 A4
VMA_MA5 P3 A5
VMA_MA6 R9 A6
VMA_MA7 R3 A7
VMA_MA8 T9 A8
VMA_MA9 R4 A9
VMA_MA10 L8 A10/AP
VMA_MA11 R8 A11
VMA_MA12 N8 A12/BC
VMA_MA13 T4 A13
T8 A14
M8 A15/BA3

VMA_BA0 M3 BA0
VMA_BA1 N9 BA1
VMA_BA2 M4 BA2

VMA_CLK1 J8 CK
VMA_CLK1# K8 CK
VMA_CKE1 K10 CKE/CKE0

VMA_ODT1 K2 ODT/ODT0
VMA_CS1# L3 CS /CS0
VMA_RAS1# J4 RAS
VMA_CAS1# K4 CAS
VMA_WE1# L4 WE

VMA_RDQS6 F4 DQSL
VMA_RDQS7 C8 DQSU

VMA_DM6 E8 DML
VMA_DM7 D4 DMU

VMA_WDQS6 G4 DQSL
VMA_WDQS7 B8 DQSU

VM_RST# T3 RESET

VMA_ZQ4 L9 ZQ/ZQ0

DQL0 F4 VMA_DQ49
DQL1 F8 VMA_DQ52
DQL2 F3 VMA_DQ50
DQL3 F9 VMA_DQ54
DQL4 H4 VMA_DQ51
DQL5 H9 VMA_DQ53
DQL6 G3 VMA_DQ48
DQL7 H8 VMA_DQ55

D8 VMA_DQ63
C4 VMA_DQ56
C9 VMA_DQ62
C3 VMA_DQ59
A8 VMA_DQ60
A3 VMA_DQ58
B9 VMA_DQ61
A4 VMA_DQ57

+1.5V_VGA

VDD#B3 B3
VDD#D10 D10
VDD#G8 G8
VDD#K3 K3
VDD#K9 K9
VDD#N2 N2
VDD#N10 N10
VDD#R2 R2
VDD#R10 R10

+1.5V_VGA

VDDQ#A2 A2
VDDQ#A9 A9
VDDQ#C2 C2
VDDQ#C10 C10
VDDQ#D3 D3
VDDQ#E10 E10
VDDQ#F2 F2
VDDQ#H3 H3
VDDQ#H10 H10

VSS#A10 A10
VSS#B4 B4
VSS#E2 E2
VSS#G9 G9
VSS#J3 J3
VSS#J9 J9
VSS#M2 M2
VSS#M10 M10
VSS#P2 P2
VSS#P10 P10
VSS#T2 T2
VSS#T10 T10

VSSQ#B2 B2
VSSQ#B10 B10
VSSQ#D2 D9
VSSQ#D9 E3
VSS#E3 E9
VSSQ#E9 F10
VSSQ#F10 G2
VSSQ#G2 G10
VSSQ#G10

NC A1
NC T1
NC A11
NC T11
NC/ODT1 J2
NC/CS1 L2
NC/CE1 J10
NC/ZQ1 L10

Should be 240 Ohms +-1%

R449 *243/F_4

+1.5V_VGA

R1 *4.99K/F_4 — VREFC_VMA1 — R9 *4.99K/F_4 — C24 *.1U/10V_4
R457 *4.99K/F_4 — VREFD_VMA1 — R455 *4.99K/F_4 — C644 *.1U/10V_4
R444 *4.99K/F_4 — VREFC_VMA2 — R447 *4.99K/F_4 — C636 *.1U/10V_4
R453 *4.99K/F_4 — VREFD_VMA2 — R452 *4.99K/F_4 — C635 *.1U/10V_4
R443 *4.99K/F_4 — VREFC_VMA3 — R446 *4.99K/F_4 — C634 *.1U/10V_4
R8 *4.99K/F_4 — VREFD_VMA3 — R7 *4.99K/F_4 — C12 *.1U/10V_4
R445 *4.99K/F_4 — VREFC_VMA4 — R448 *4.99K/F_4 — C633 *.1U/10V_4
R456 *4.99K/F_4 — VREFD_VMA4 — R454 *4.99K/F_4 — C643 *.1U/10V_4

VMA_CLK1 — R6 *40.2/F_4 — VMA_CLK1_COMM — C8 *.01U/16V_4 — R4 *40.2/F_4 — VMA_CLK1#
VMA_CLK0 — R5 *40.2/F_4 — VMA_CLK0_COMM — C11 *.01U/16V_4 — R3 *40.2/F_4 — VMA_CLK0#

+1.5V_VGA

C33 C623 C648 C641 C615 C618 C610 C630 *1U/6.3V_4
C651 C617 C620 C640 C616 C619 C614 C99 *1U/10V_4
C6 C631 C626 C665 C638 C637 C628 C650 *1U/6.3V_4
C632 C645 C639 C611 C647 C613 C612 C5 *1U/6.3V_4

C824 C825 C822 C820 C821 C826 C827 C823 *1U/6.3V_4

DV2...ADD +1.5V_VGA CAP

C22 C657 C4 C27 C14 *10U/6.3V_6S
C44 C699 C3 C100 C19 *10U/6.3V_6S

[15,18,20,27,39] +1.5V_VGA

NB5

PROJECT : LG3/5 Muxless & UMA
Quanta Computer Inc.

Size	Document Number	Rev
Custom	VRAM-A (DDR3 BGA96)	2A
Date: Wednesday, March 07, 2012	Sheet 19 of 42	

CHANNEL B: 256MB/512MB DDR3

[15] VMB_DQ[63..0]
[15] VMB_DM[7..0]
[15] VMB_WDQS[7..0]
[15] VMB_RDQS[7..0]

VRAM7 / VRAM3 / VRAM4 / VRAM8

100-BALL SDRAM DDR3
K4W1G1646E-HC12

Should be 240 Ohms +-1%

R467 243/F_4 — R22 243/F_4 — R56 243/F_4 — R497 243/F_4

R465 4.99K/F_4 / R466 4.99K/F_4 / C676 .1U/10V_4 — VREFC_VMB1
R464 4.99K/F_4 / R463 4.99K/F_4 / C666 .1U/10V_4 — VREFD_VMB1
R24 4.99K/F_4 / R23 4.99K/F_4 / C49 .1U/10V_4 — VREFC_VMB2
R48 4.99K/F_4 / R50 4.99K/F_4 / C114 .1U/10V_4 — VREFD_VMB2
R59 4.99K/F_4 / R66 4.99K/F_4 / C177 .1U/10V_4 — VREFC_VMB3
R98 4.99K/F_4 / R99 4.99K/F_4 / C212 .1U/10V_4 — VREFD_VMB3
R495 4.99K/F_4 / R496 4.99K/F_4 / C723 .1U/10V_4 — VREFC_VMB4
R483 4.99K/F_4 / R484 4.99K/F_4 / C700 .1U/10V_4 — VREFD_VMB4

VMB_CLK0 — R20 40.2/F_4 — VMB_CLK0_COMM — C48 .01U/16V_4 — R21 40.2/F_4 — VMB_CLK0#
VMB_CLK1 — R100 40.2/F_4 — VMB_CLK1_COMM — C213 .01U/16V_4 — R101 40.2/F_4 — VMB_CLK1#

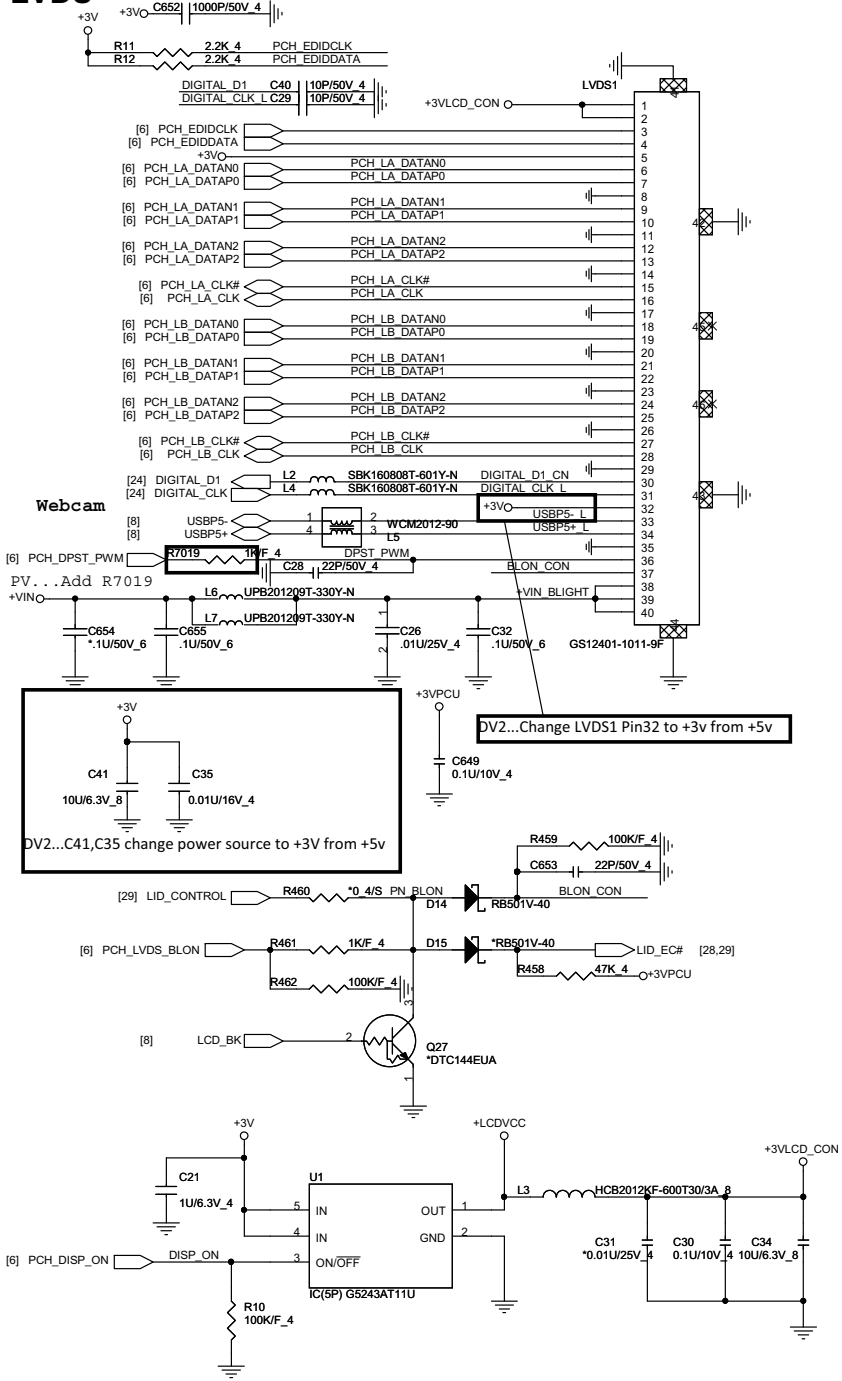
+1.5V_VGA decoupling: C47 C663 C682 C66 C662 C50 C660 C46 (1U/6.3V_4); C658 C679 C661 C667 C84 C664 C659 C51 (1U/6.3V_4); C216 C211 C718 C725 C726 C214 C707 C101 (1U/6.3V_4); C727 C724 C215 C92 C712 C728 C711 C680 (1U/6.3V_4); C53 C71 C187 C56 C45 C183 C189 C135 C156 C147 (10U/6.3V_6S)

[15,18,19,27,39] +1.5V_VGA

PROJECT :	LG3/5 Muxless & UMA
Quanta Computer Inc.	
Size: Custom	Document Number: VRAM-B (DDR3 BGA96) — Rev: 2A
Date: Wednesday, March 07, 2012	Sheet 20 of 42

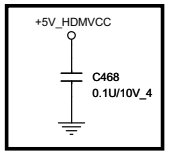
NB5

LVDS



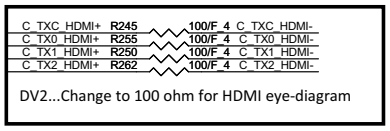
HDMI

DV2...Add 0.1U CAP at +5V_HDMVCC for EMI



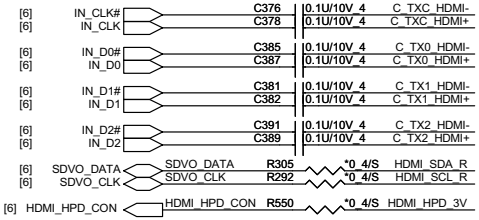
Close connector < 50 mil

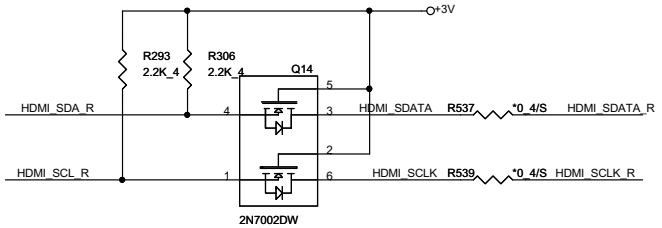
EMI



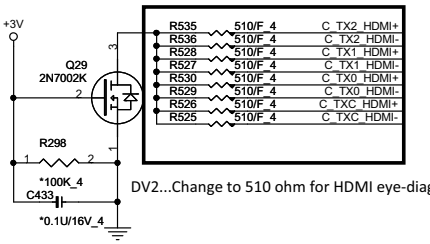
DV2...Change to 100 ohm for HDMI eye-diagram

For Muxless/UMA HDMI function





Close connector < 50 mil



DV2...Change to 510 ohm for HDMI eye-diagram

+5VCRT

[7,10,22,23,24,26,28,38] +5V
[2,6,7,8,9,10,12,13,14,16,22,23,24,25,26,27,28,29,34,36,38,40] +3V

NB5

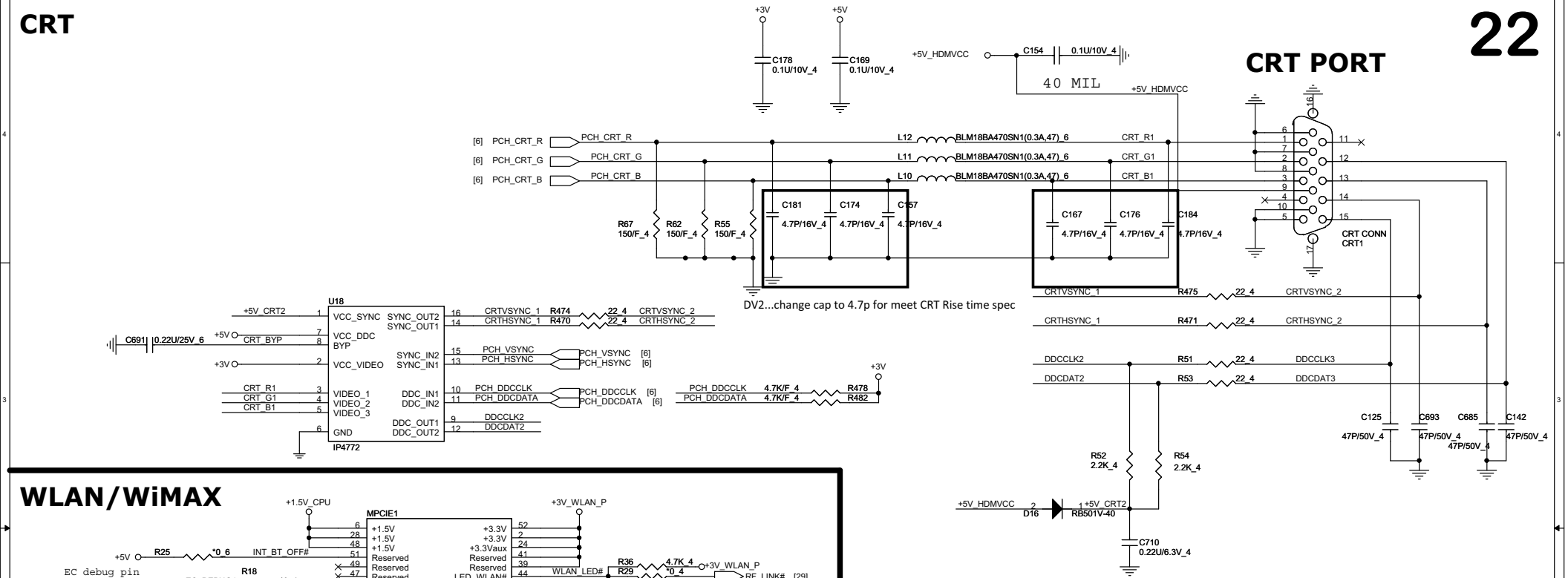
PROJECT : LG3/5 Muxless & UMA
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDMI and LVDS	2A
Date: Wednesday, March 07, 2012	Sheet 21 of 42	

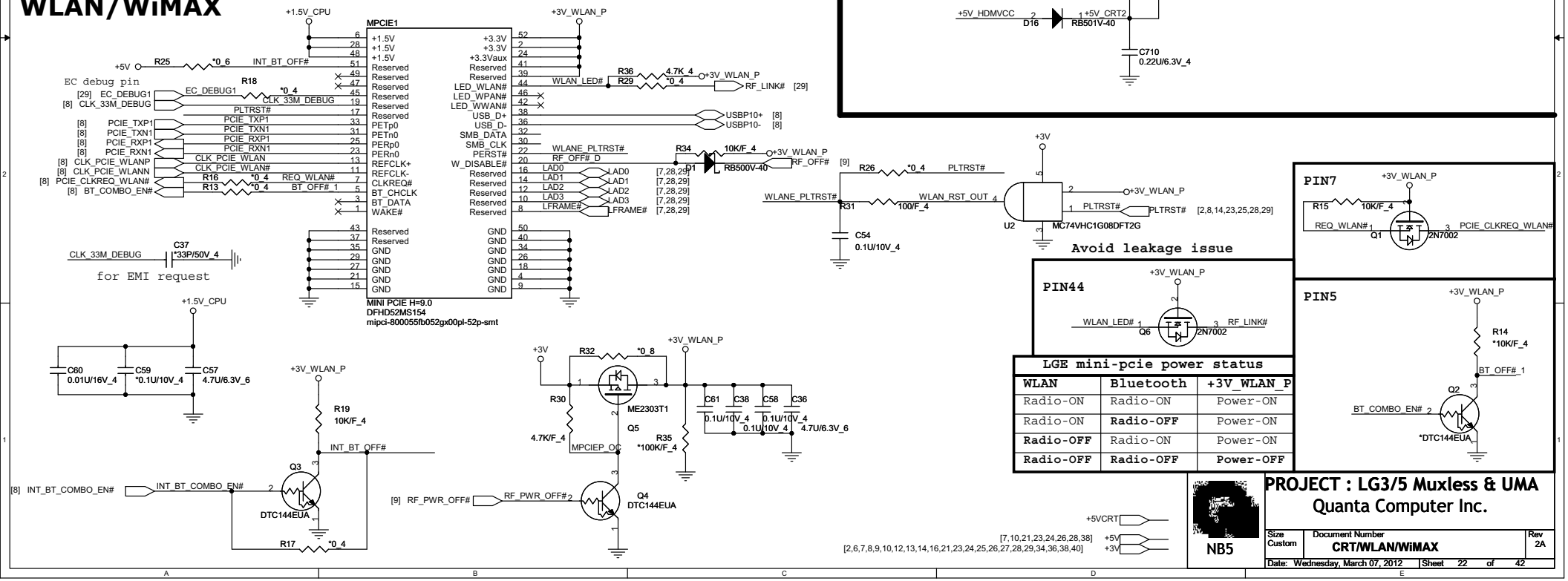
CRT

22

CRT PORT



WLAN/WiMAX

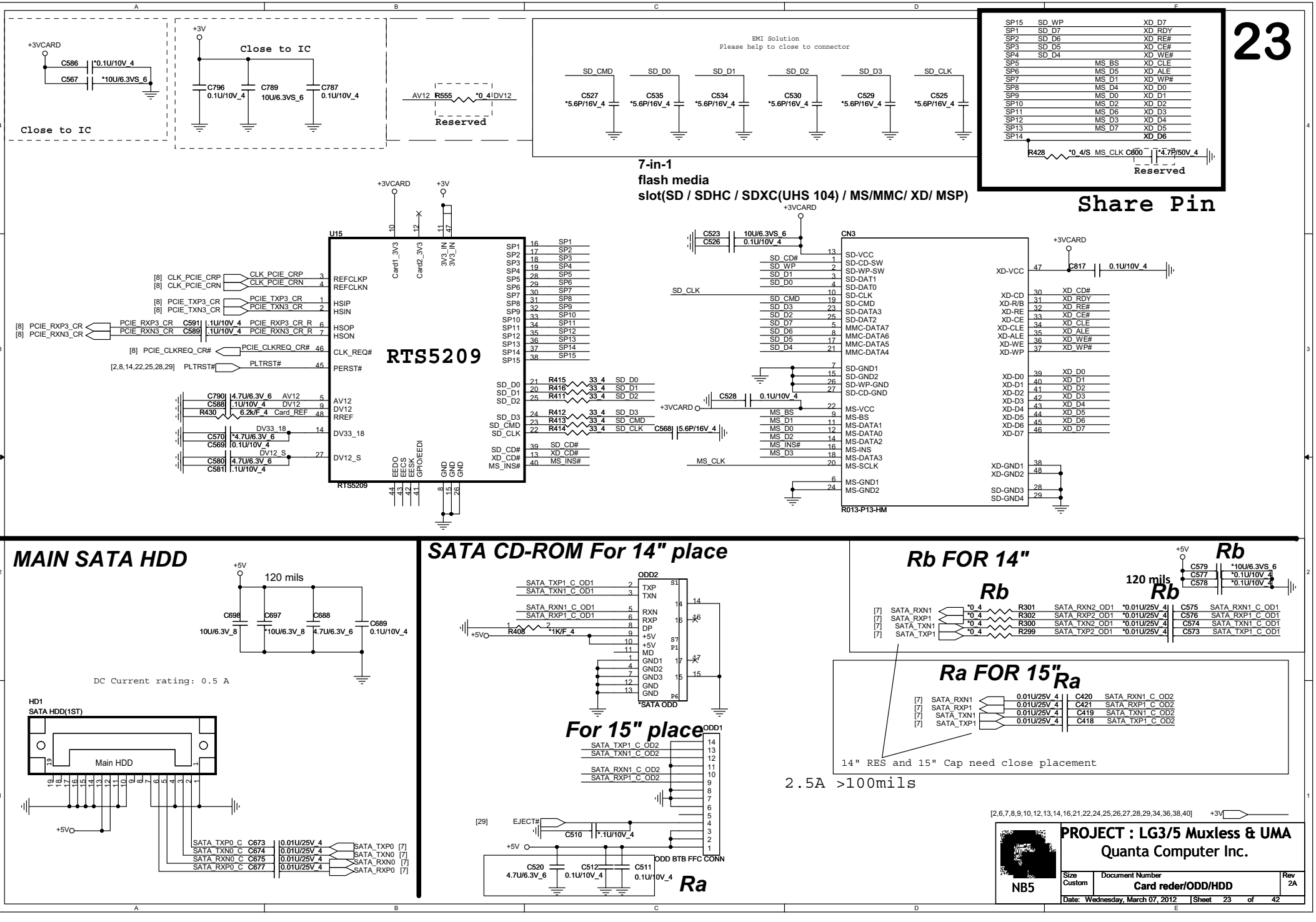


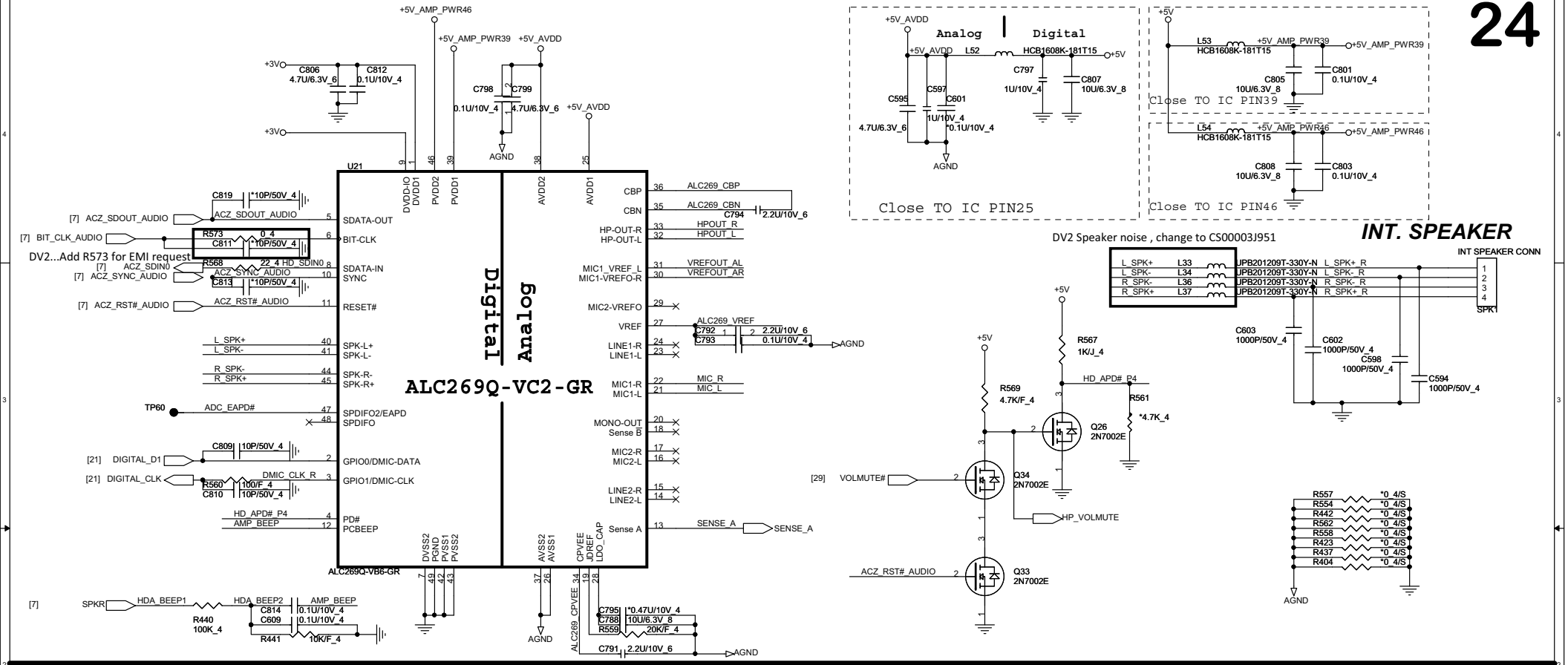
LGE mini-pcie power status		
WLAN	**Bluetooth**	**+3V_WLAN_P**
Radio-ON	Radio-ON	Power-ON
Radio-ON	**Radio-OFF**	Power-ON
Radio-OFF	Radio-ON	Power-ON
Radio-OFF	**Radio-OFF**	**Power-OFF**

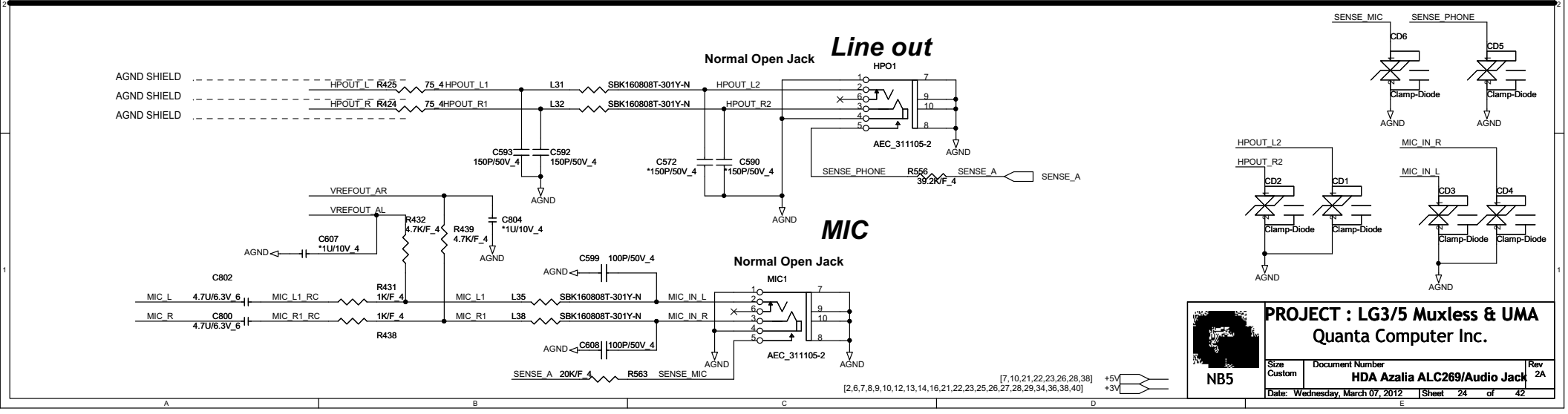
NB5

PROJECT : LG3/5 Muxless & UMA
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT/WLAN/WiMAX	2A
Date: Wednesday, March 07, 2012	Sheet 22 of 42	


+3VCARD
C586 *0.1U/10V_4
C567 *10U/6.3VS_6
Close to IC
+3V
Close to IC
C796 0.1U/10V_4
C789 10U/6.3VS_6
C787 0.1U/10V_4
AV12 R555 *0_4 DV12
Reserved
EMI Solution
Please help to close to connector
SD_CMD SD_D0 SD_D1 SD_D2 SD_D3 SD_CLK
C527 *5.6P/16V_4
C535 *5.6P/16V_4
C534 *5.6P/16V_4
C530 *5.6P/16V_4
C529 *5.6P/16V_4
C525 *5.6P/16V_4
SP15 SD_WP XD_D7
SP1 SD_D7 XD_RDY
SP2 SD_D6 XD_RE#
SP3 SD_D5 XD_CE#
SP4 SD_D4 XD_WE#
SP5 MS_BS XD_CLE
SP6 MS_D5 XD_ALE
SP7 MS_D1 XD_WP#
SP8 MS_D4 XD_D0
SP9 MS_D0 XD_D1
SP10 MS_D2 XD_D2
SP11 MS_D6 XD_D3
SP12 MS_D3 XD_D4
SP13 MS_D7 XD_D5
SP14 XD_D6
R428 *0_4/S MS_CLK C600 *4.7P/50V_4
Reserved
7-in-1
flash media
slot(SD / SDHC / SDXC(UHS 104) / MS/MMC/ XD/ MSP)
Share Pin
U15
RTS5209
+3VCARD
+3V
Card1_3V3
Card2_3V3
3V3_IN
REFCLKP
REFCLKN
HSIP
HSIN
HSOP
HSON
CLK_REQ#
PERST#
AV12
DV12
RREF
DV33_18
DV12_S
EEDO
EECS
EESK
GPIO/EEDI
GND
[8] CLK_PCIE_CRP
[8] CLK_PCIE_CRN
[8] PCIE_TXP3_CR
[8] PCIE_TXN3_CR
[8] PCIE_RXP3_CR
[8] PCIE_RXN3_CR
PCIE_RXP3_CR_R
PCIE_RXN3_CR_R
[8] PCIE_CLKREQ_CR#
[2,8,14,22,25,28,29] PLTRST#
C591 .1U/10V_4
C589 .1U/10V_4
C790 4.7U/6.3V_6
C588 .1U/10V_4
R430 6.2k/F_4 Card_REF
C570 *4.7U/6.3V_6
C569 0.1U/10V_4
C580 4.7U/6.3V_6
C581 .1U/10V_4
SD_D0 SD_D1 SD_D2 SD_D3 SD_CMD SD_CLK
R415 33_4
R416 33_4
R411 33_4
R412 33_4
R413 33_4
R414 33_4
C568 5.6P/16V_4
SD_CD# XD_CD# MS_INS#
CN3
R013-P13-HM
C523 10U/6.3VS_6
C526 0.1U/10V_4
C528 0.1U/10V_4
C817 0.1U/10V_4
SD-VCC SD-CD-SW SD-WP-SW SD-DAT1 SD-DAT0 SD-CLK SD-CMD SD-DATA3 SD-DAT2 MMC-DATA7 MMC-DATA6 MMC-DATA5 MMC-DATA4
SD-GND1 SD-GND2 SD-WP-GND SD-CD-GND
MS-VCC MS-BS MS-DATA1 MS-DATA0 MS-DATA2 MS-INS MS-DATA3 MS-SCLK
MS-GND1 MS-GND2
SD-GND3 SD-GND4
XD-VCC XD-CD XD-R/B XD-RE XD-CE XD-CLE XD-ALE XD-WE XD-WP
XD-D0 XD-D1 XD-D2 XD-D3 XD-D4 XD-D5 XD-D6 XD-D7
XD-GND1 XD-GND2
MAIN SATA HDD
+5V
120 mils
C698 10U/6.3V_8
C697 *10U/6.3V_8
C688 4.7U/6.3V_6
C689 0.1U/10V_4
DC Current rating: 0.5 A
HD1
SATA HDD(1ST)
Main HDD
SATA_TXP0_C C673 0.01U/25V_4
SATA_TXN0_C C674 0.01U/25V_4
SATA_RXN0_C C675 0.01U/25V_4
SATA_RXP0_C C677 0.01U/25V_4
SATA_TXP0 [7]
SATA_TXN0 [7]
SATA_RXN0 [7]
SATA_RXP0 [7]
SATA CD-ROM For 14" place
ODD2
SATA_TXP1_C_OD1
SATA_TXN1_C_OD1
SATA_RXN1_C_OD1
SATA_RXP1_C_OD1
R408 *1K/F_4
*SATA ODD
For 15" place
ODD1
SATA_TXP1_C_OD2
SATA_TXN1_C_OD2
SATA_RXN1_C_OD2
SATA_RXP1_C_OD2
[29] EJECT#
C510 *.1U/10V_4
C520 4.7U/6.3V_6
C512 0.1U/10V_4
C511 0.1U/10V_4
ODD BTB FFC CONN
Rb FOR 14"
Rb
120 mils
[7] SATA_RXN1
[7] SATA_RXP1
[7] SATA_TXN1
[7] SATA_TXP1
R301 SATA_RXN2_OD1 *0.01U/25V_4 C575 SATA_RXN1_C_OD1
R302 SATA_RXP2_OD1 *0.01U/25V_4 C576 SATA_RXP1_C_OD1
R300 SATA_TXN2_OD1 *0.01U/25V_4 C574 SATA_TXN1_C_OD1
R299 SATA_TXP2_OD1 *0.01U/25V_4 C573 SATA_TXP1_C_OD1
C579 *10U/6.3VS_6
C577 *0.1U/10V_4
C578 *0.1U/10V_4
Ra FOR 15"
Ra
C420 SATA_RXN1_C_OD2
C421 SATA_RXP1_C_OD2
C419 SATA_TXN1_C_OD2
C418 SATA_TXP1_C_OD2
14" RES and 15" Cap need close placement
2.5A >100mils
[2,6,7,8,9,10,12,13,14,16,21,22,24,25,26,27,28,29,34,36,38,40] +3V
PROJECT : LG3/5 Muxless & UMA
Quanta Computer Inc.
NB5
Size Custom
Document Number Card reder/ODD/HDD
Rev 2A
Date: Wednesday, March 07, 2012
Sheet 23 of 42





NB5	PROJECT : LG3/5 Muxless & UMA Quanta Computer Inc.	
	Size: Custom	Document Number: HDA Azalia ALC269/Audio Jack
	Date: Wednesday, March 07, 2012	Sheet 24 of 42

placed 0.1U within 200 mil close to AR8151

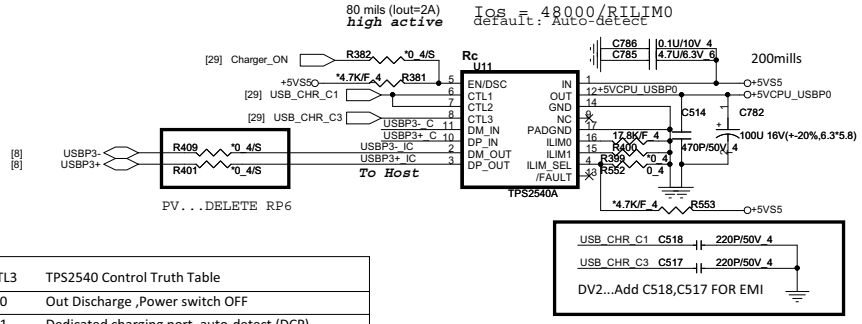
placed VDD33 CAP within 400 mil close to AR8151

PLACE NEAR LAN IC PIN6

PV...Change C474 to 0 ohm FOR EMI

PV...ADD RES from GND to LAN_AGND for EMI

Charger USB

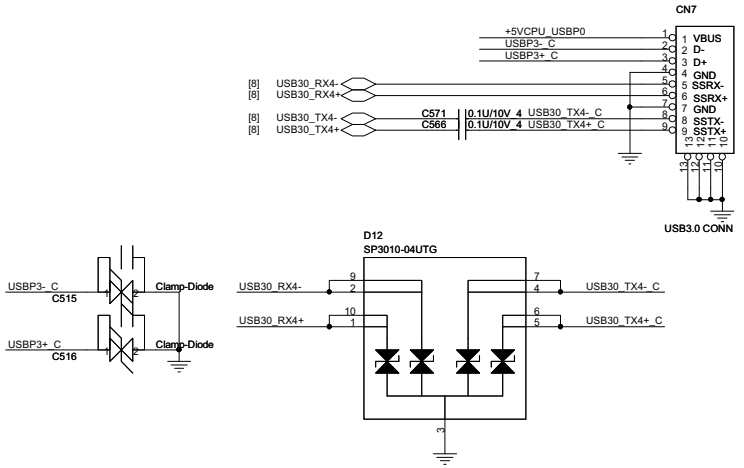


CTL1	CTL2	CTL3	TPS2540 Control Truth Table
0	0	0	Out Discharge ,Power switch OFF
0	X	1	Dedicated charging port, auto-detect (DCP)
X	1	0	Standard downstream port, USB 2.0 Mode.(SDP)
1	1	1	Charging downstream port, BC1.2 (draft).(CDP)

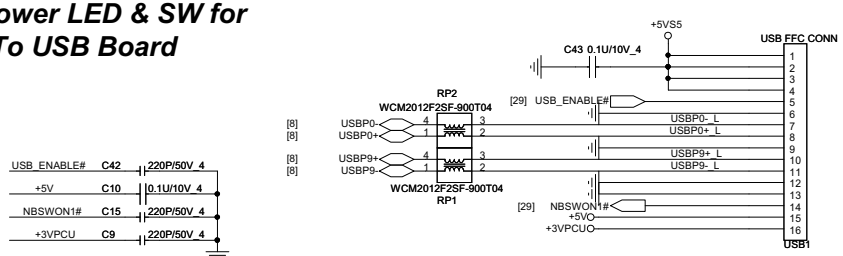
Detect device to Charge:AUTO Detect		
Fast Charge	S0	S3
Enable	CDP	DCP
Disabled	SDP	SDP

Current Battery Capacity	Always-on Charge	S4/S5	
		AC Mode	DC Mode
>Low battery level	Enable	DCP	DCP
	Disabled	OFF	OFF
<=Low battery level	Enable	DCP	OFF
	Disabled	OFF	OFF

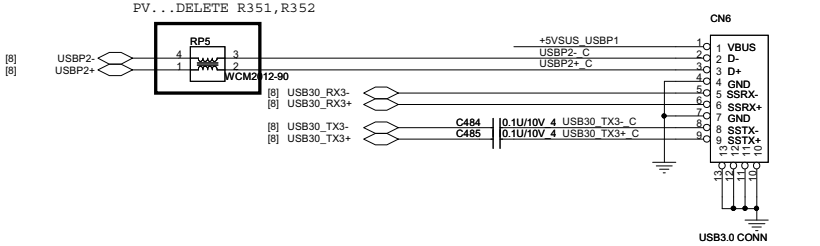
USB3.0/USB2.0 x1 COMBO/Charger Port



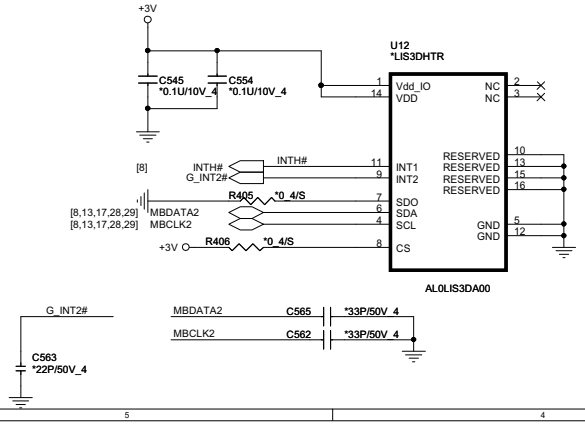
USB / Power LED & SW for 14"/15"To USB Board

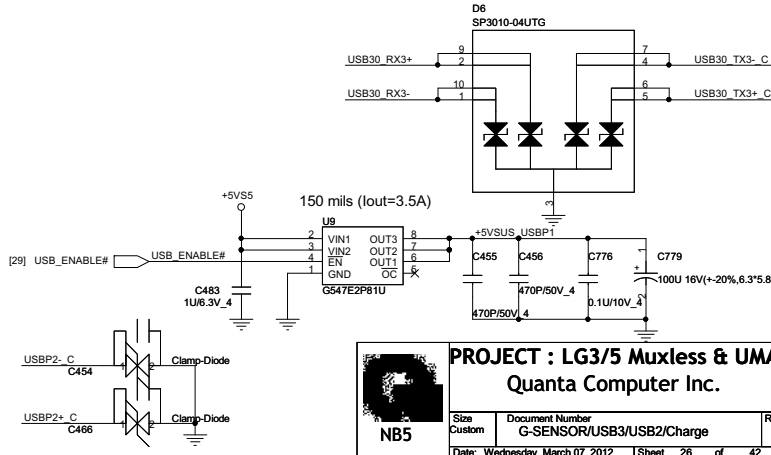


USB3.0/USB2.0 x1 COMBO



Accelerometer Sensor

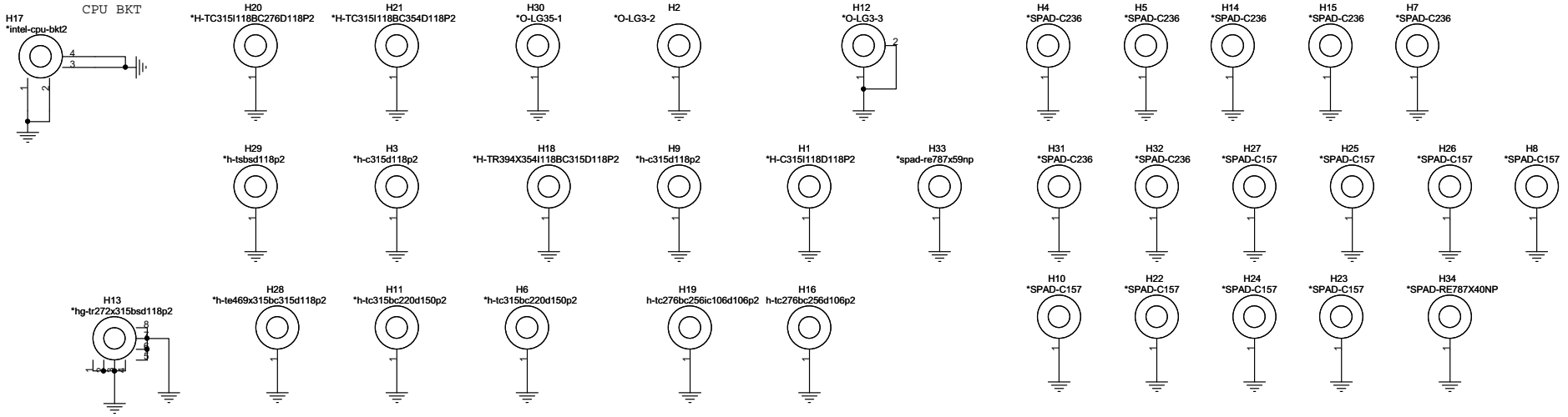




PROJECT : LG3/5 Muxless & UMA
Quanta Computer Inc.

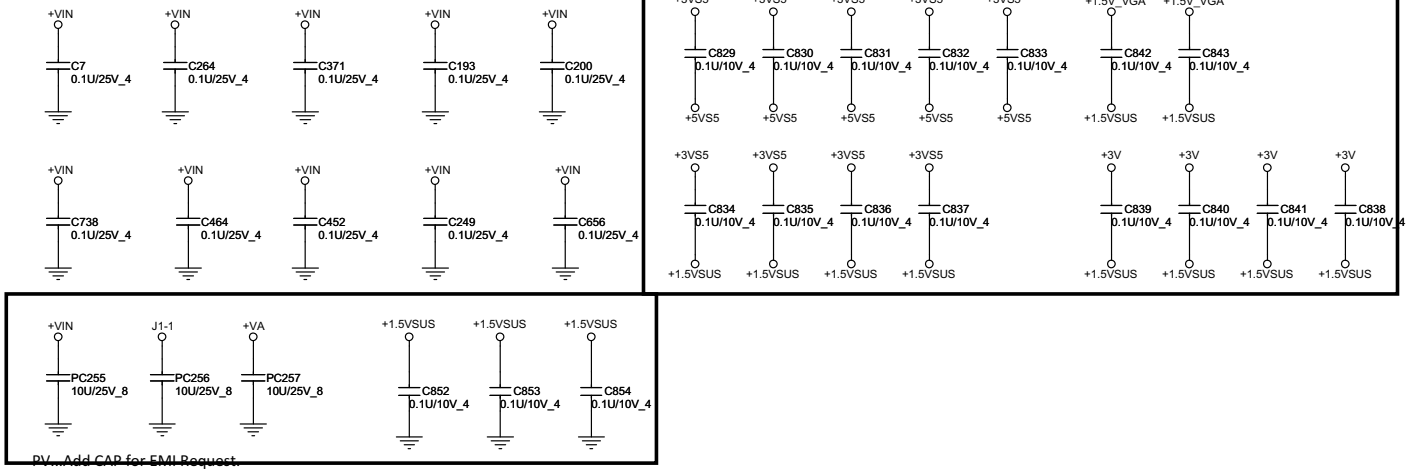
Size	Document Number	Rev
Custom	G-SENSOR/USB3/USB2/Charge	2A
Date: Wednesday, March 07, 2012	Sheet 26 of 42	

Hole



EMI CAP

DV2...Add stitch cap between power plane for EMI Request.



PV...Add CAP for EMI Request.

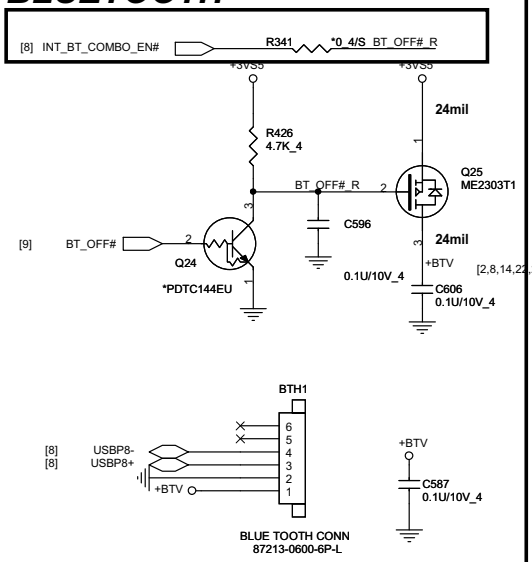
[38,39] +12VALW
[7,10,21,22,23,24,26,28,38] +5V
[2,6,7,8,9,10,12,13,14,16,21,22,23,24,25,26,28,29,34,36,38,40] +3V

NB5

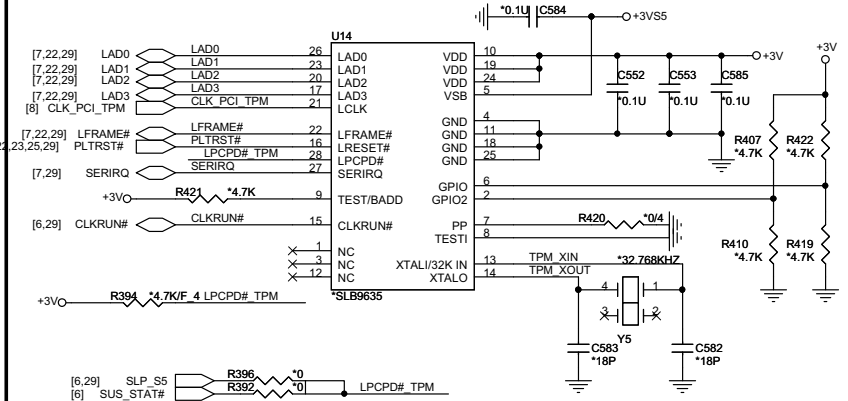
PROJECT : LG3/5 Muxless & UMA
Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB 3.0 Controller (VIA_VL801)	2A
Date: Wednesday, March 07, 2012	Sheet 27 of 42	

BLUETOOTH

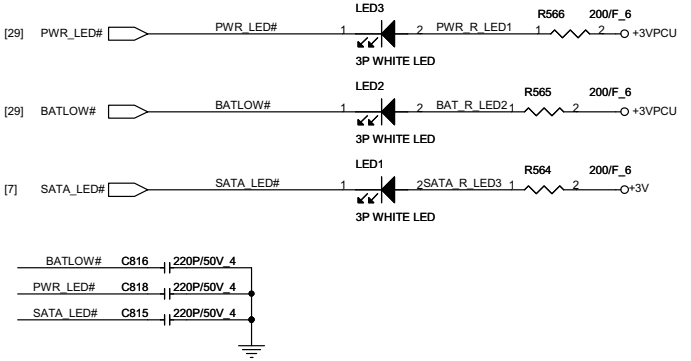


TPM (1.2)

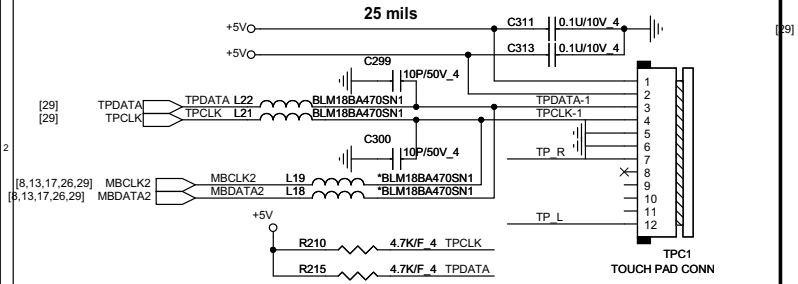


LED

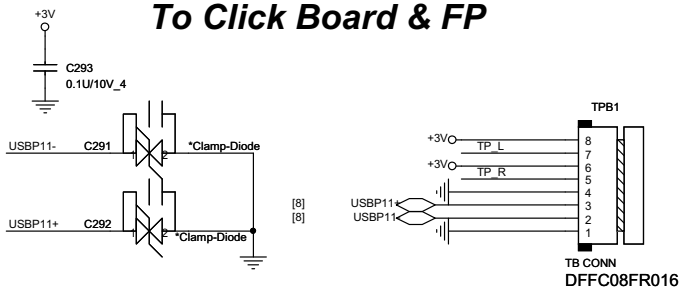
10 mils (250mA)



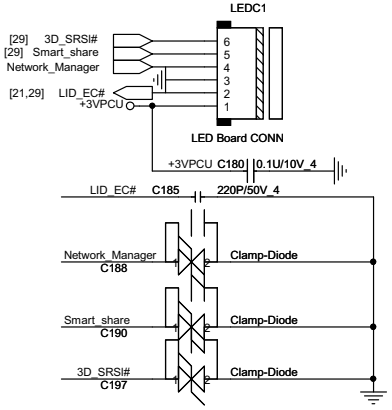
TOUCH PAD CONNECTOR
To Touch Pad



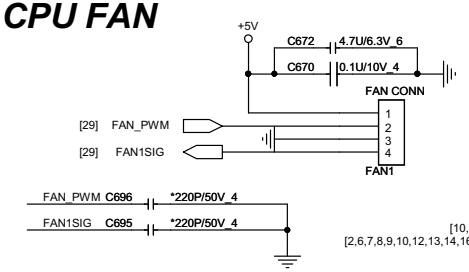
TP Button CONNECTOR
To Click Board & FP



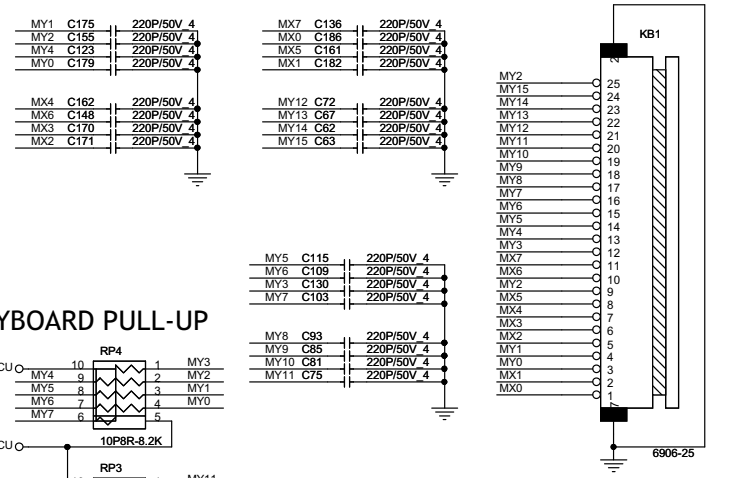
To LID Function Board



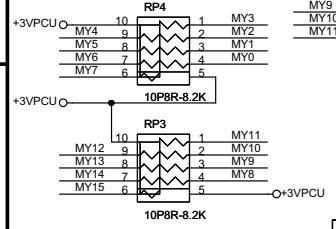
CPU FAN

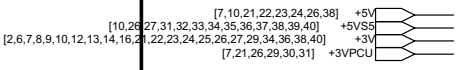


KEYBOARD Con.



KEYBOARD PULL-UP





NB5

PROJECT : LG3/5 Muxless & UMA
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BT/FR/LED/TP/TPM	2A
Date: Wednesday, March 07, 2012	Sheet 28 of 42	

DV2...Stuff C560,C548,C559,C547 for EMI request

LAD0 C560 22P
LAD1 C548 22P
LAD2 C559 22P
LAD3 C547 22P
PLTRST# C555 *22P

Layout Note:
Place all capacitors close to IT8502N.

+3VPCU 12 MILS
C556 0.1U/10V_4
C491 0.1U/10V_4
C470 0.1U/10V_4
C508 0.1U/10V_4
C519 0.1U/10V_4
C557 0.1U/10V_4

+3V_RTC R397 *0/short_4 +VCC_RTC
C558 0.1U/10V_4

+VCC_RTC R391 *0_4
+3V_ECACC L28 BK1608HS220-T +3VPCU
C471 1U/6.3V_4
C465 1000P/50V_4
IT8502_AGND IT8502_AGND
+3v_STBY L30 BK1608HS121-T +3VPCU
C522 0.1U/10V_4
C549 0.1U/10V_4
R387 *0_4/S
+3V +3VPCU

R395 470K/J_4 +3VPCU
EC_WRST
C550 0.1U/10V_4

MBCLK R374 10K/J_4 +3VPCU
MBDATA R375 10K/J_4

TPCLK R349 *10K/J_4 +3V
TPDATA R348 *10K/J_4
MBCLK2 R376 10K/J_4
MBDATA2 R377 10K/J_4
3D_SRSI# R343 10K/F_4
Network_Manager R338 10K/F_4
FAN1SIG R372 10K/F_4
Smart_share R336 10K/J_4

H_PROCHOT#_Q R333 *0_4/S H_PROCHOT# [2,36]
+3VPCU
H_PROCHOT#_EC
Q17 2N7002E
R350 100K/J_4
R388 10K/J_4
NBSWON1#
C546 0.1U/10_4

PWR_LED# [28]
PWR_LED
Q22 2N7002E
BATLOW# [28]
BATLOW
Q18 2N7002E

U10
IT8518/HX
IT8518E

LPC
LAD0 [7,22,28]
LAD1 [7,22,28]
LAD2 [7,22,28]
LAD3 [7,22,28]
LPCRST#/WUI4/GPD2 [2,8,14,22,23,25,28] PLTRST#
LPCCLK [8] CLK_33M_KBC
LFRAME# [7,22,28] LFRAME#
LPCPD#/WUI6/GPE6 [6,28] SLP_S5#

GPIO
EGCLK/WUI27/GPE3 BATLOW
EGCS#/WUI26/GPE2 VRON [36]
EGAD/WUI25/GPE1 PM_SLP_A# TP39
KSO16/SMOSI/GPC3 EC_PWROK [6]
KSO17/SMISO/GPC5 M_POWEROK TP40
L80HLAT/BAO/WUI24/GPE0 SUSON [32]
L80LLAT/WUI7/GPE7 PM_SLP_LAN# TP45
SBUSY/GPG1/ID7 MBATLED0 TP41
HMOSIGPH6/ID6 H_SI R362 *0_4/S PCH_SPI_SI [7]
HMISO/GPH5/ID5 H_SO R359 *0_4/S PCH_SPI_SO [7]
HSCK/GPH4/ID4 H_CLK R357 *0_4/S PCH_SPI_CLK [7]
HSCE#/WUI19/GPH3/ID3 H_SCE# R358 *0_4/S PCH_SPI_CS1# [7] R355 *0_4 PCH_SPI_CS0# [7]
CTX1/WUI18/GPH2/SMDAT3/ID2 MAINON [30,32,34,35,38]
CRX1/WUI17/GPH1/SMCLK3/ID1 RF_LINK# [22]
CLKRUN#/WUI16/GPH0/ID0 CLKRUN# [6,28]

PS/2
PS2DAT0/TMB1/GPF1
PS2CLK0/TMB0/GPF0
PS2DAT2/WUI21/GPF5 TPDATA [28]
PS2CLK2/WUI20/GPF4 TPCLK [28]

SM_BUS
SMCLK2/WUI22/GPF6/PECI EC_PECI_R R380 *0_4/S EC_PECI [2]
SMDAT2/WUI23/GPF7 CAP_INT TP42
SMCLK0/GPB3 MBCLK [30]
SMDAT0/GPB4 MBDATA [30] For Battery charge/charge
SMCLK1/GPC1 MBCLK2 [8,13,17,26,28]
SMDAT1/GPC2 MBDATA2 [8,13,17,26,28] For PCH SMB/DDR Thermal IC/VGA/G-SENSOR

UART
DAC4/DCD0#/GPJ4
DSR0#/GPG6
GINT/CTS0#/GPD5
PS2DAT1/RTS0#/GPF3
DAC5/RIG0#/GPJ5
PS2CLK1/DTR0#/GPF2
RXD/SIN0/GPB0
TXD/SOUT0/GPB1

FLASH
GPG0
FSCK
FMISO
FMOSI
FSCE#
SSCE0#/GPG2

PWM
PWM0/GPA0 LAN_POWER [38]
PWM1/GPA1 Num LK T4
PWM2/GPA2 AC_PRESENT TP44
PWM3/GPA3 SATA5GP_EC TP43
PWM4/GPA4 FAN_PWM [28]
PWM5/GPA5 SUS_PWR_ACK [6]
PWM6/SSCK/GPA6 VOLMUTE# [24]
PWM7/GPA7 USB_CHR_C2 T3
TACH0/GPD6 FAN1SIG [28]
TACH1/TMA1/GPD7 3VS5_ON [31]
TMR0/WUI2/GPC4 SUSC# [6]
TMR1/WUI3/GPC6 5VS5_ON [31]

KBMX
KSO0/PD0
KSO1/PD1
KSO2/PD2
KSO3/PD3
KSO4/PD4
KSO5/PD5
KSO6/PD6
KSO7/PD7
KSO8/ACK#
KSO9/BUSY
KSO10/PE
KSO11/ERR#
KSO12/SLCT
KSO13
KSO14
KSO15
KSI0/STB#
KSI1/AFD#
KSI2/INIT#
KSI3/SLIN#
KSI4
KSI5
KSI6
KSI7

WAKE UP
C551 0.1U/10V_4
PWRSW/GPE4 NBSWON1# NBSWON1# [26]
RI1#/WUI0/GPD0 LID_EC# [21,28]
RI2#/WUI1/GPD1 ACIN [30]
WUI5/GPE5 SUSB# [6]
RING#/PWRFAIL#/CK32KOUT/LPCRST#/GPB7 PWR_LED

A/D D/A
ADC0/GPI0 CB_ID
ADC1/GPI1 Smart_share [28]
ADC2/GPI2 SYS_I [30]
ADC3/GPI3 AD_AIR [30]
ADC4/WUI28/GPI4 TEMP_MBAT [30]
ADC5/WUI29/GPI5 Network_Manager [28]
ADC6/WUI30/GPI6 3D_SRSI# [28]
ADC7/WUI31/GPI7 Setvpro

CLOCK
CK32K
CK32KE
DAC0/GPJ0 USB_CHR_C1 [26]
DAC1/GPJ1 DGPU_PWROK [8,9,39,40]
DAC2/GPJ2 VFAN T2
DAC3/GPJ3 D4 RB501V-40 DNBSWON# [6]
R327 10K/F_4 +3VS5

D9 RB501V-40 [9] EC_A20GATE [7,28] SERIRQ
D11 RB501V-40 [9] SIO_EXT_SMI# [9] SIO_EXT_SCI#
D8 RB501V-40
EC_WRST
D10 RB501V-40 [9] EC_RCIN# T5

[30] D/C# [6] RSMRST#
H_PROCHOT#_EC [26] Charger_ON

DV2...GPU_PROCHOT#,GPIO5_PROCHOT# to GPU and ADD R365
[16] GPU_PROCHOT# *0_4 R365 GPU_PROCHOT#_R
CB/LG
[26] USB_CHR_C2 EC_GPXA6
[31,32,33,34,35] HWPG
[21] LID_CONTROL
D5 need to close PCH. TP38
[7] ACZ_SDOUT GPIO33_E_R
[22] EC_DEBUG1
D7 RB501V-40
[26] USB_ENABLE#

EC_SCK EC_SCK_L L8042 SBY100505T-121Y-N Add L8042 for EMI request
C500 22P_50v
EC_SO EC_SI EC_CE#
[23] EJECT# [28] MY[0..15]
[28] MX[0..7]

DV2 ...DGPU_PWROK Pull down to disable GPU Thermal for UMA M/B

DGPU_PWROK R7018 Rh *10K/J_4

Platform	ADC	Select
LG3/LG5	0V	Rg

Board ID Select Pin
Rg R344 10K_4 CB_ID R345 *10K_4 +3VPCU

Platform	ADC	Select
LG3/LG5	0V	Rg

LG/CB Select Pin
Rb R346 *10K_4 CB/LG R347 10K_4 Ra +3VPCU

	Select
LG	Ra
CB	Rb

Vpro Select Pin
Re R342 10K_4 Setvpro R335 *10K_4 Rf +3VPCU

	Vpro Select
Vpro	Rf
Non-Vpro	Re

thermal shutdown circuit
EC_WRST
EC_CT_UP R393 *4.7K/F_4 +1.05V
C564 220P/50V_4
PV Change
Q23 *MMBT3904-7-F PM_THRMTRIP# [2,9]

U16 Placement TOP side

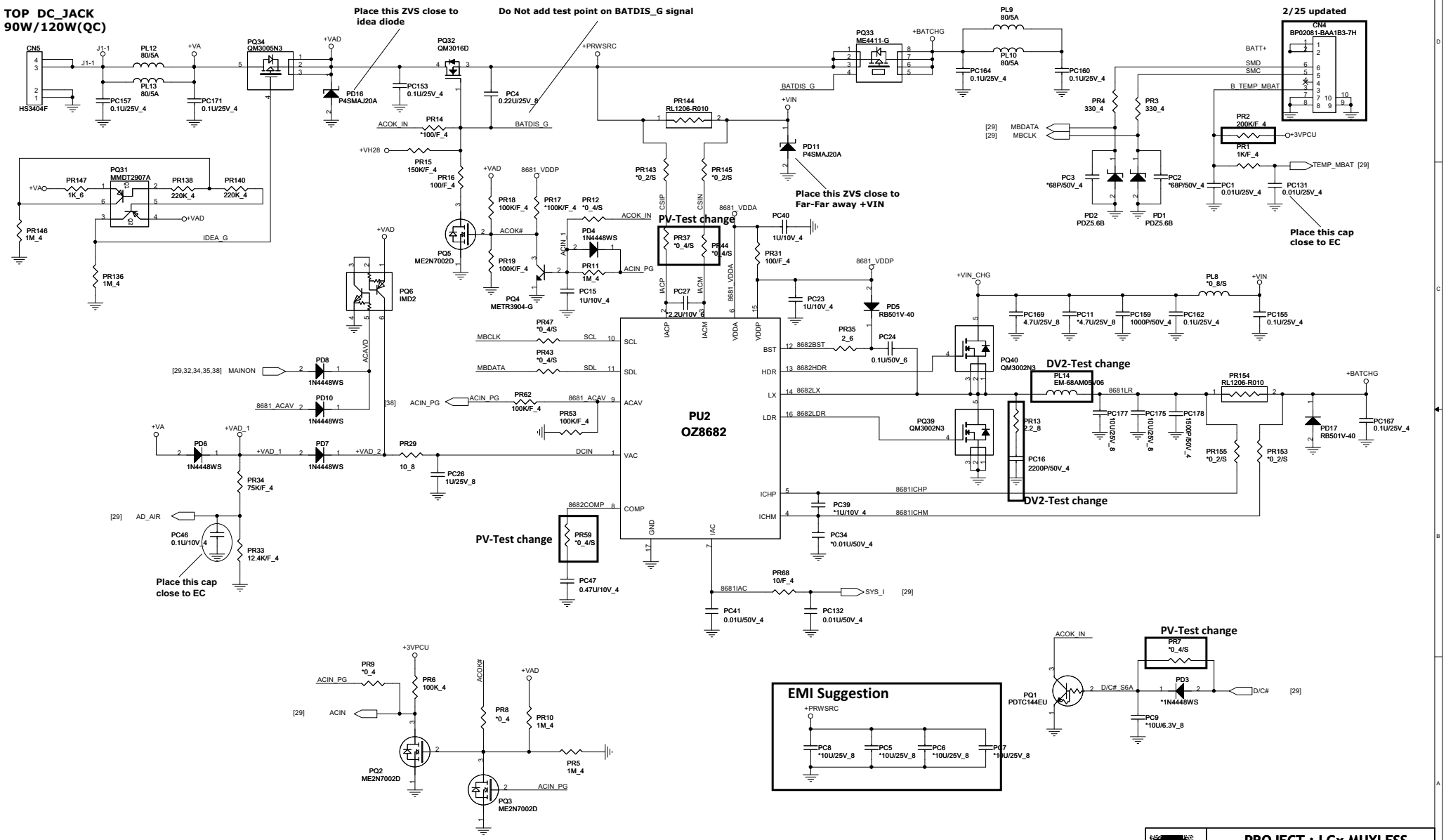
Vender	Size	P/N
EON	4MB	AKE39ZN0Q02 (EN25Q32B-104HIP)
AMIC	4MB	AKE39F-0800 (A25LQ32AM-F/Q)
Socket		DFHS08FS023

Add C845 C844 C828 for EMI request
EC_CE# C845 22P
EC_SI_R C844 22P
EC_SO C828 22P

EC_SCK_R R434 *47_4 C604 *22P
U16
EC_CE# EC_SCK R435 47/J_4 EC_SCK_R EC_SI R433 47/J_4 EC_SI_R EC_SO R418 15/J_4 EC_SO_R
CE# SCK SI SO WP# HOLD# VDD VSS
R417 10K/J_4 +3VPCU
R436 10K/J_4
C605 0.1U/10V_4
SPI Flash Socket

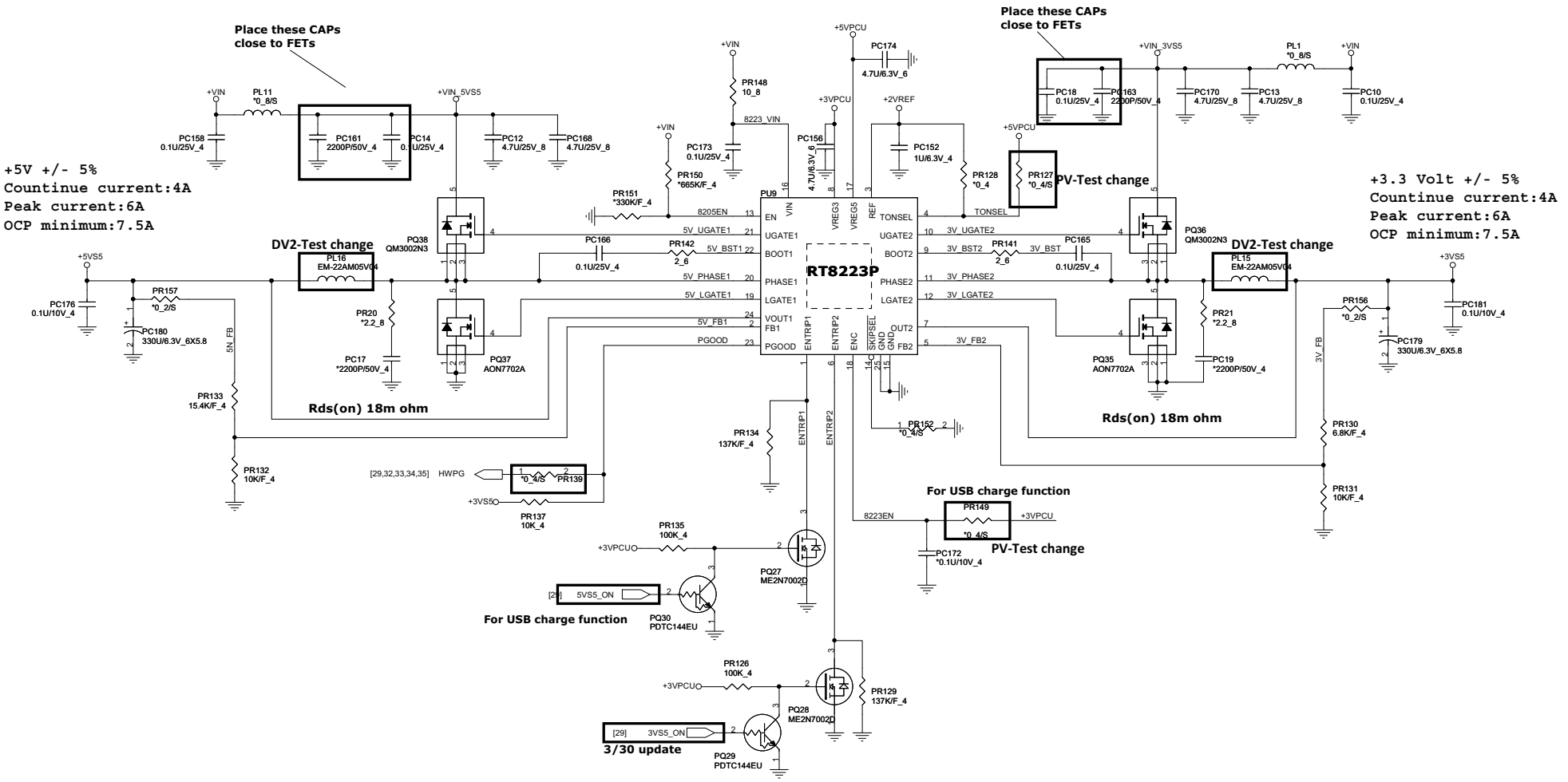
L29 BK1608HS121-T IT8502_AGND
C561 0.1U/10V_4 IT8502_AGND
[6,7,10] +3V_RTC
[6,7,8,9,10,27,28,31,34,35,38,39] +3VS
[2,6,7,8,9,10,12,13,14,16,21,22,23,24,25,26,27,28,34,36,38,40] +3V
[7,21,26,28,30,31] +3VPCU

NB5
PROJECT : LG3/5 Muxless & UMA
Quanta Computer Inc.
Size Custom | Document Number IT8515/HX/FLASH | Rev 2A
Date: Wednesday, March 07, 2012 | Sheet 29 of 42

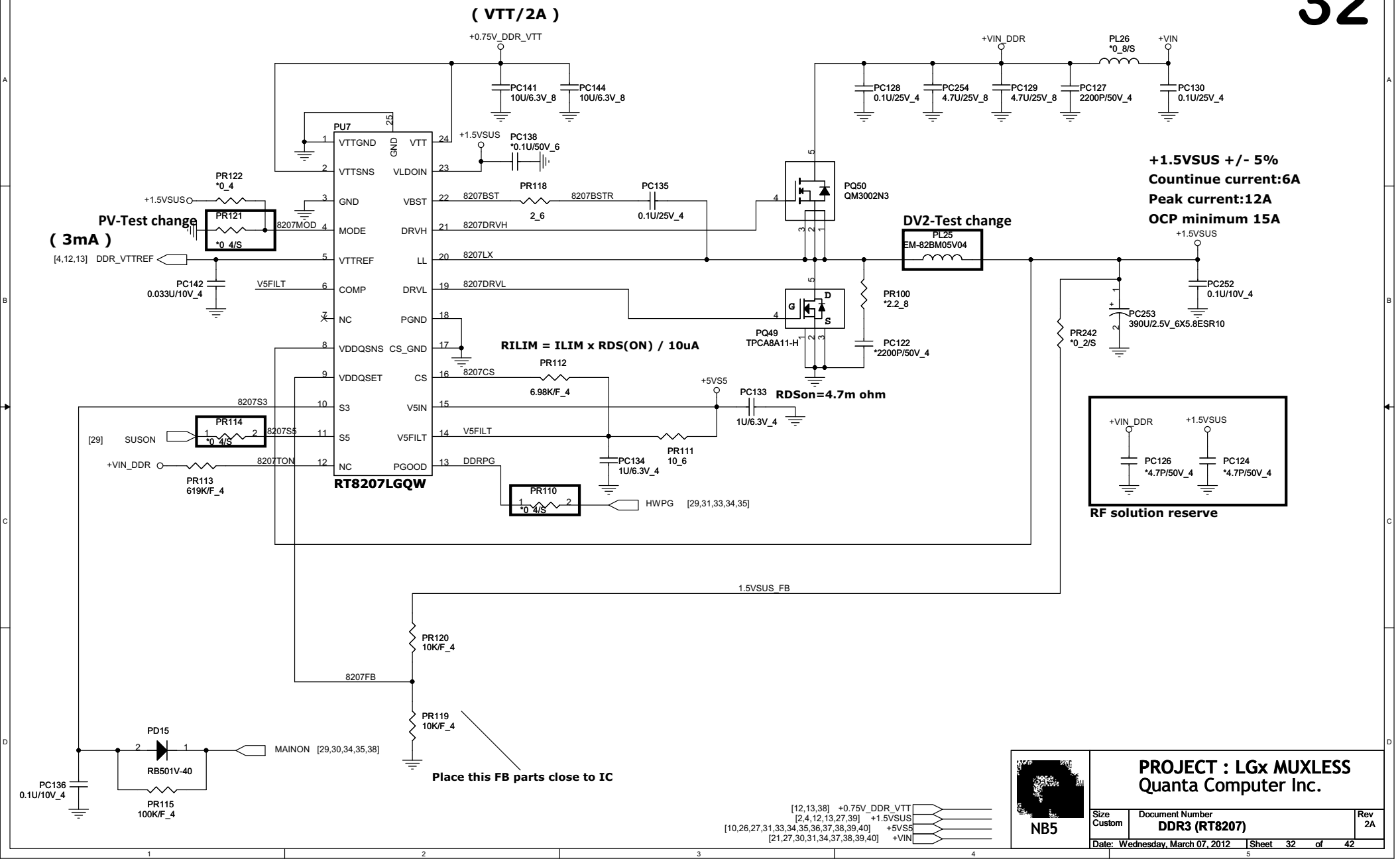

TOP DC_JACK
90W/120W(QC)
Place this ZVS close to idea diode
Do Not add test point on BATDIS_G signal
2/25 updated
Place this ZVS close to Far-Far away +VIN
PV-Test change
Place this cap close to EC
DV2-Test change
PU2
OZ8682
EMI Suggestion
PROJECT : LGx MUXLESS
Quanta Computer Inc.
Charger (OZ8681)
NB5
Date: Wednesday, March 07, 2012
Sheet 30 of 42

DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

LG2_DIS only

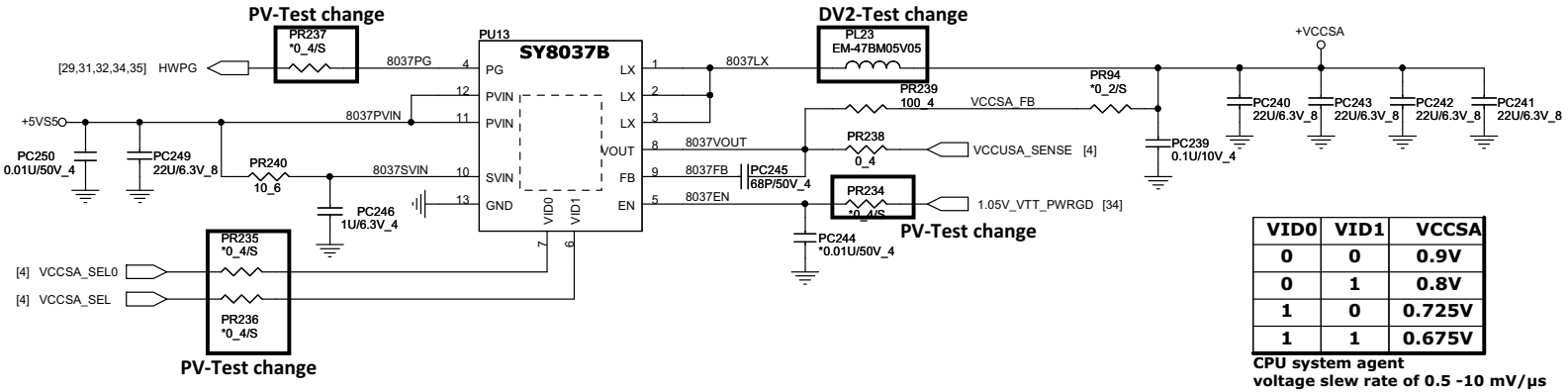


NB5	PROJECT : LGx MUXLESS Quanta Computer Inc.	
Size: Custom	Document Number: 3/5VS5 (RT8223M)	Rev: 2A
Date: Wednesday, March 07, 2012	Sheet 31 of 42	



NB5	PROJECT : LGx MUXLESS Quanta Computer Inc.	
Size: Custom	Document Number: DDR3 (RT8207)	Rev: 2A
Date: Wednesday, March 07, 2012	Sheet 32 of 42	

+VCCSA Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7A



VID0	VID1	VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

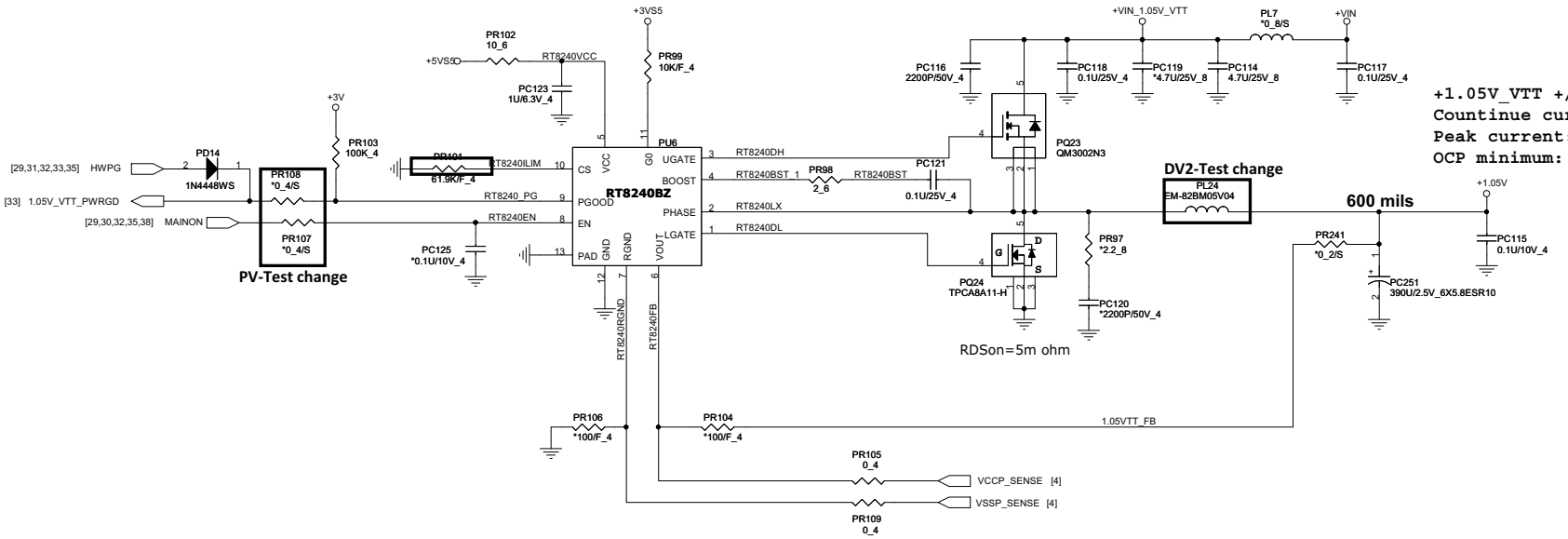
CPU system agent
voltage slew rate of 0.5 -10 mV/µs

NB5

PROJECT : LGx MUXLESS
Quanta Computer Inc.

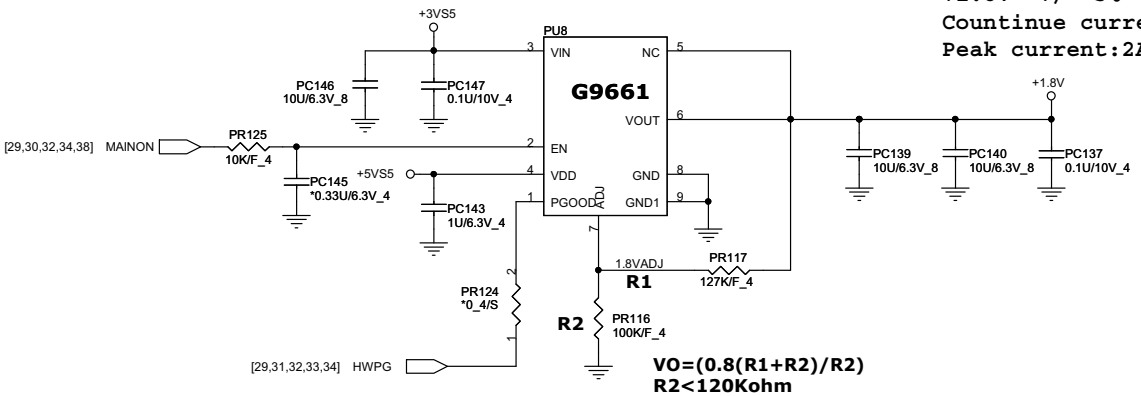
Size	Document Number	Rev
B	VCCSA (RT8241A)	2A

Date: Wednesday, March 07, 2012 | Sheet 33 of 42



+1.05V_VTT +/- 5%
Countinue current:10A
Peak current: 12A
OCP minimum: 14.5A

NB5	PROJECT : LGx MUXLESS Quanta Computer Inc.	
Size: Custom	Document Number: +1.05V(RT8240B)	Rev: 2A
Date: Wednesday, March 07, 2012	Sheet 34 of 42	

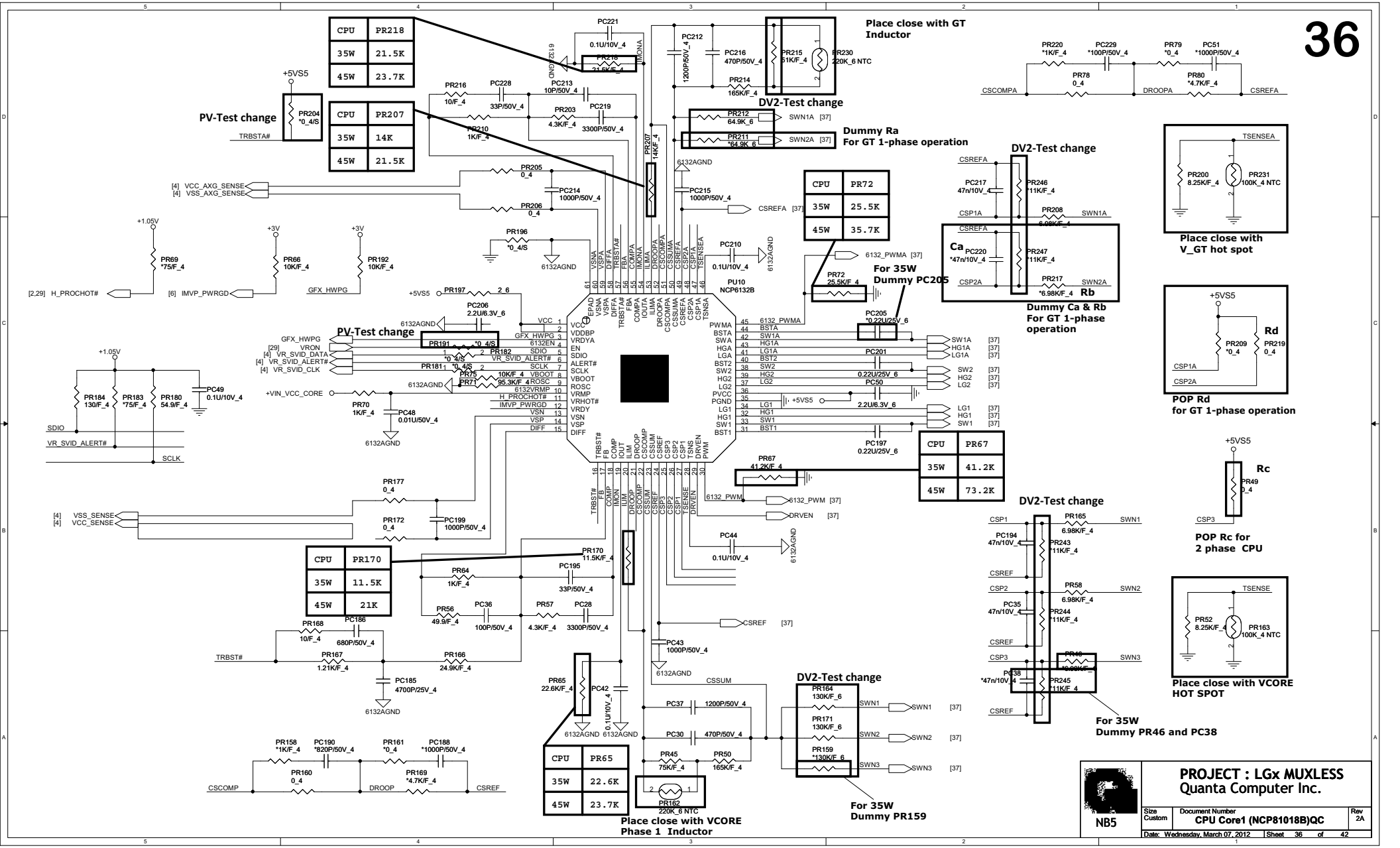


NB5

PROJECT : LGx MUXLESS
Quanta Computer Inc.

Size	Document Number	Rev
B	+1.8V (G9661)	2A

Date: Wednesday, March 07, 2012 | Sheet 35 of 42


CPU PR218
35W 21.5K
45W 23.7K
CPU PR207
35W 14K
45W 21.5K
PV-Test change
PR204 *0_4/S
TRBSTA#
+5VS5
Place close with GT Inductor
DV2-Test change
PR212 64.9K_6
PR211 *64.9K_6
SWN1A [37]
SWN2A [37]
Dummy Ra
For GT 1-phase operation
CPU PR72
35W 25.5K
45W 35.7K
6132_PWMA [37]
For 35W
Dummy PC205
PR72 25.5K/F_4
PU10
NCP6132B
PC205 *0.22U/25V_6
PC201 0.22U/25V_6
PC50 2.2U/6.3V_6
PC197 0.22U/25V_6
CPU PR67
35W 41.2K
45W 73.2K
PR67 41.2K/F_4
6132_PWM [37]
DRVEN [37]
PC44 0.1U/10V_4
CPU PR170
35W 11.5K
45W 21K
PR170 11.5K/F_4
CSREF [37]
PC43 1000P/50V_4
CSSUM
PR65 22.6K/F_4
PC42 0.1U/10V_4
CPU PR65
35W 22.6K
45W 23.7K
PR162 220K_6 NTC
Place close with VCORE
Phase 1 Inductor
PC37 1200P/50V_4
PC30 470P/50V_4
PR45 75K/F_4
PR50 165K/F_4
DV2-Test change
PR164 130K/F_6
PR171 130K/F_6
PR159 *130K/F_6
SWN1 [37]
SWN2 [37]
SWN3 [37]
For 35W
Dummy PR159
DV2-Test change
PR165 6.98K/F_4
PR243 *11K/F_4
PR58 6.98K/F_4
PR244 *11K/F_4
PR245 *11K/F_4
For 35W
Dummy PR46 and PC38
PR220 *1K/F_4
PC229 *100P/50V_4
PR79 *0_4
PC51 *1000P/50V_4
PR78 0_4
PR80 *4.7K/F_4
CSCOMPA
DROOPA
CSREFA
PR200 8.25K/F_4
PR231 100K_4 NTC
TSENSEA
Place close with V_GT hot spot
DV2-Test change
PC217 47n/10V_4
PR246 *11K/F_4
PC220 *47n/10V_4
PR247 *11K/F_4
PR208 SWN1A
PR217 *6.98K/F_4 Rb
Ca
Dummy Ca & Rb
For GT 1-phase operation
PR209 *0_4
PR219 0_4
Rd
POP Rd
for GT 1-phase operation
Rc
PR49 0_4
POP Rc for
2 phase CPU
PR52 8.25K/F_4
PR163 100K_4 NTC
TSENSE
Place close with VCORE
HOT SPOT
PR158 *1K/F_4
PC190 *820P/50V_4
PR161 *0_4
PC188 *1000P/50V_4
PR160 0_4
PR169 *4.7K/F_4
CSCOMP
DROOP
CSREF
PROJECT : LGx MUXLESS
Quanta Computer Inc.
NB5
Size Custom
Document Number CPU Core1 (NCP81018B)QC
Rev 2A
Date: Wednesday, March 07, 2012
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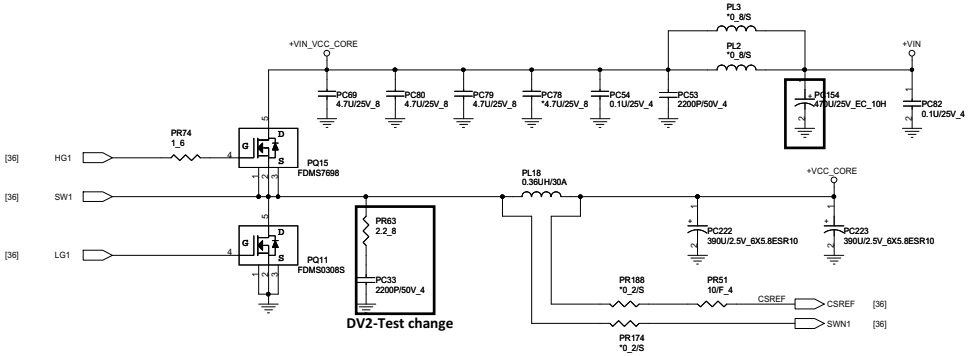
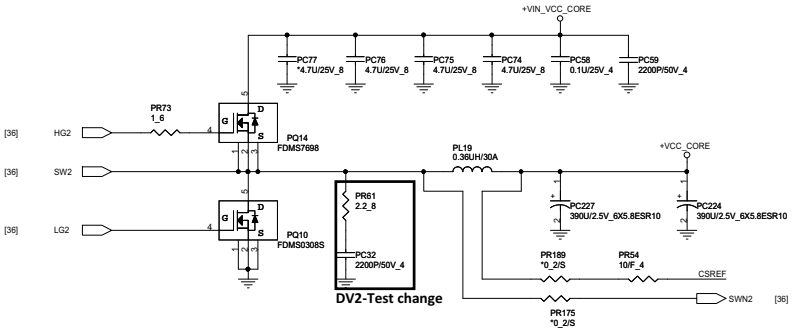
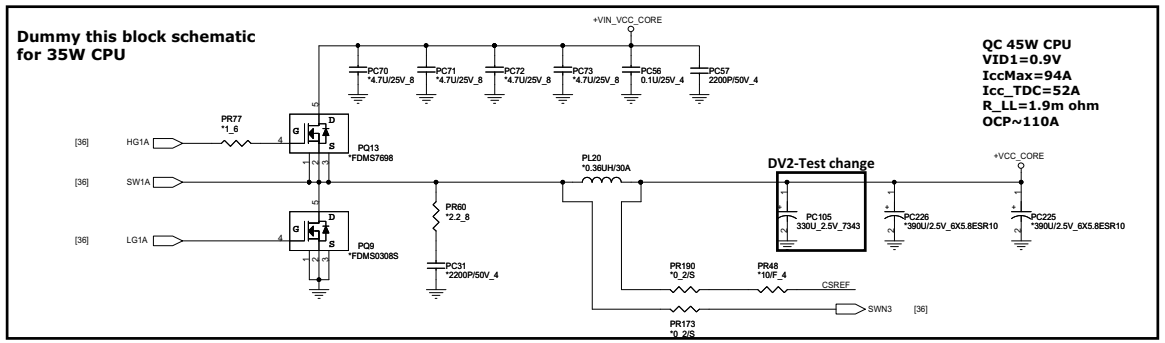
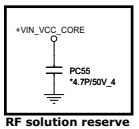
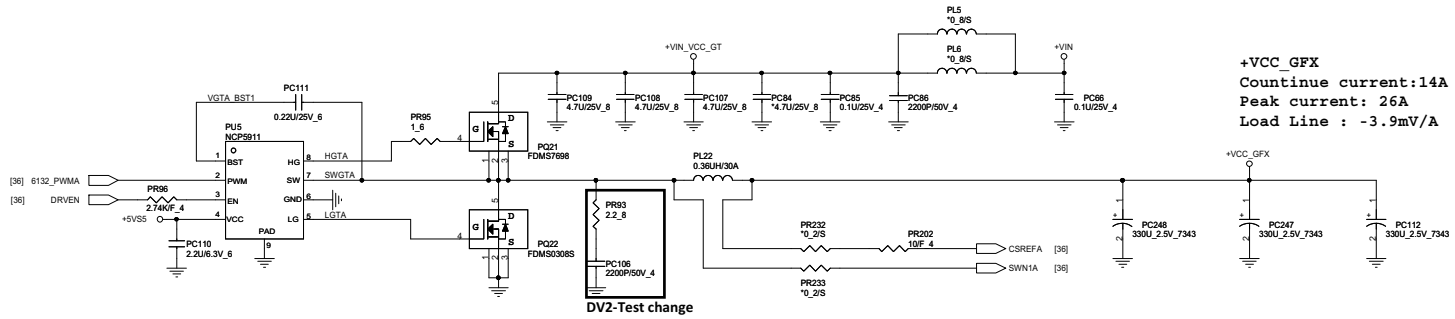


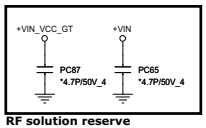


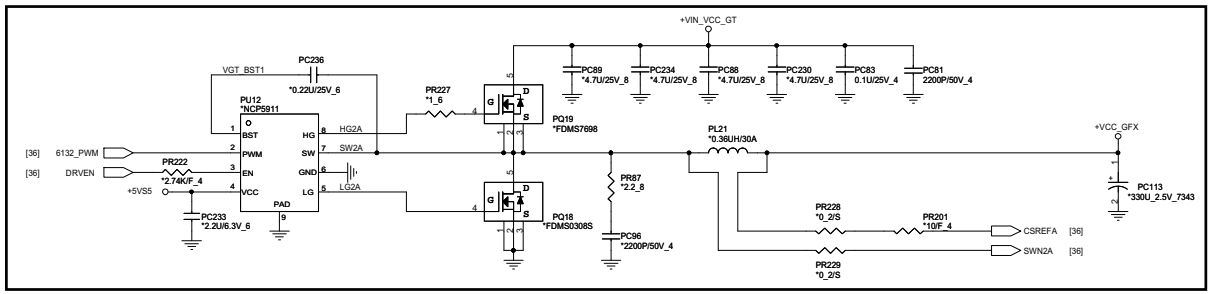




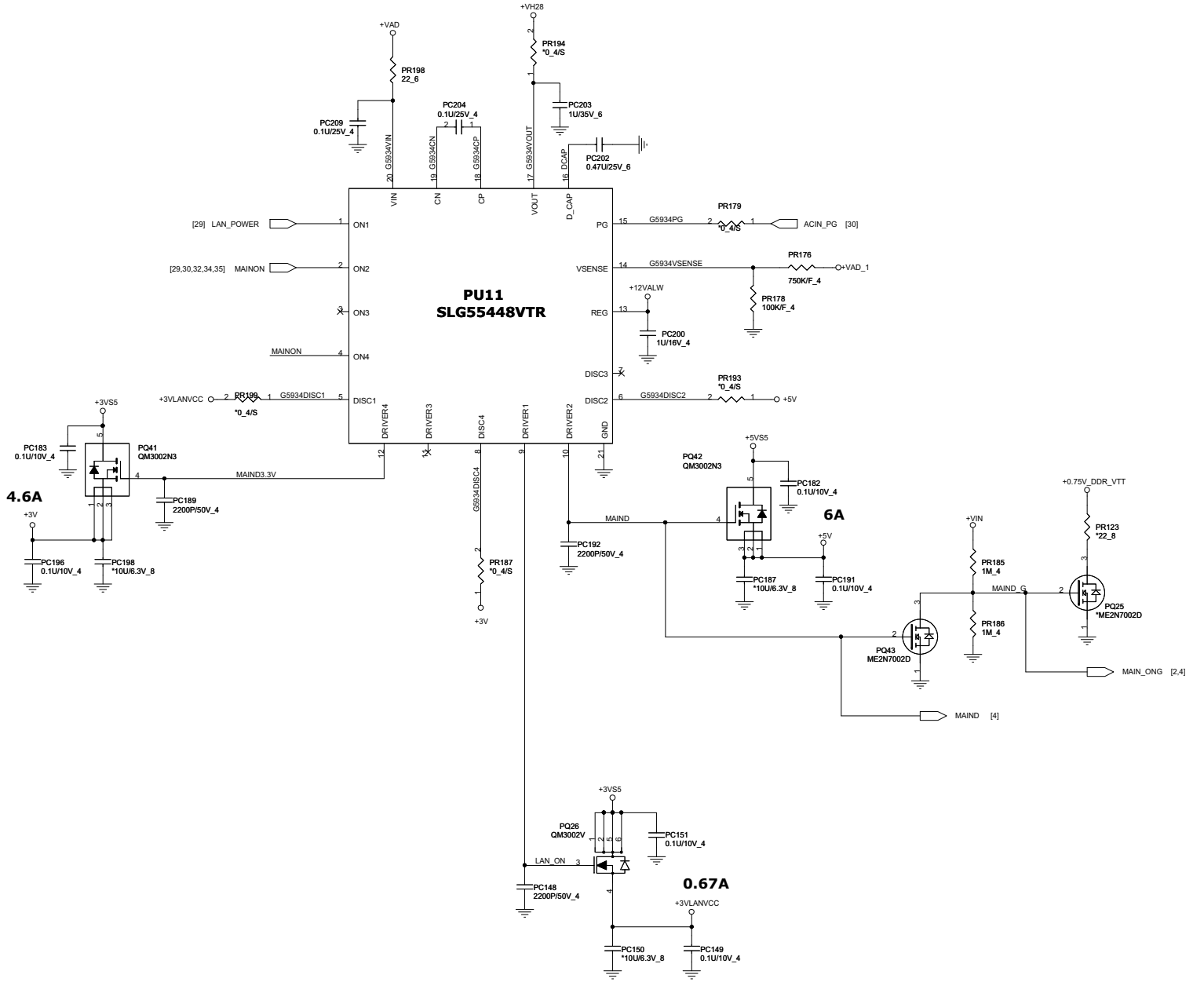


+VCC_GFX
Countinue current:14A
Peak current: 26A
Load Line : -3.9mV/A





NB5	PROJECT : LGx MUXLESS Quanta Computer Inc.	
Size: C	Document Number: CPU Core2 (NCP5911)QC	Rev: 2A
Date: Wednesday, March 07, 2012	Sheet 37 of 42	



[12,13,32] +0.75V_DDR_VTT
[7,25] +3VLANVCC
[2,4,12,13,27,32,39] +1.5VSUS
[30] +BATCHG
[39] +12VALW
[10,26,27,31,32,33,34,35,36,37,39,40] +5VS5

[6,7,8,9,10,27,28,29,31,34,35,39] +3VS5
[30] +VAD_1
[30] +VH28
[4,7,10,35] +1.8V
[21,27,30,31,32,34,37,39,40] +VIN
[7,10,21,22,23,24,26,28] +5V
[30] +VA

NB5

PROJECT : LGx MUXLESS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Dis-charge IC (G5934)	2A
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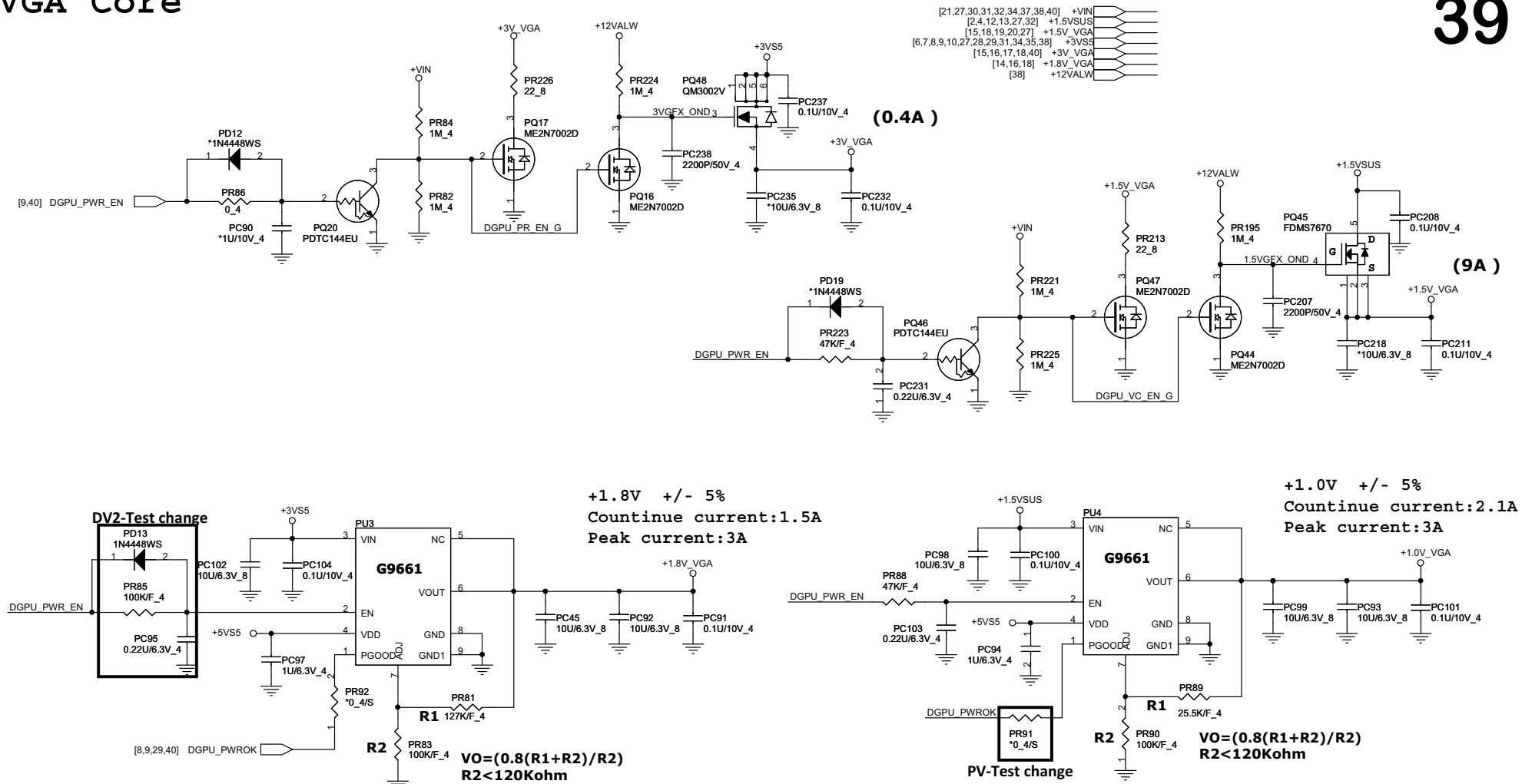
VGA Core



NB5

PROJECT : LGx MUXLESS
Quanta Computer Inc.

Size	Document Number	Rev
B	+VGA POWER	2A

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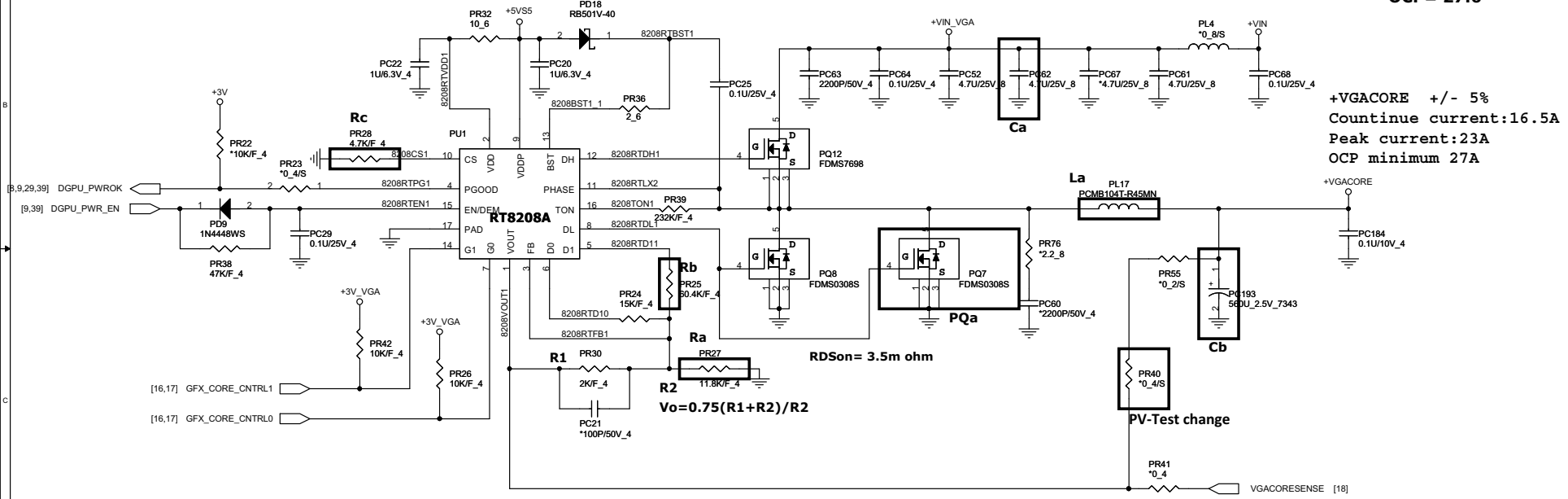
VGA Core

	Seymour	Thames
Ca	X	4.7U/25V_8
Cb	330U/2V	560U/2V
PQa	X	FDMS0308S
La	1U/15A	0.45U/25A
Ra	10K-ohm	11.8K-ohm
Rb	10K-ohm	60.4K-ohm
Rc	7.5K-ohm	4.7K-ohm

Seymour-XT 64bit
Irms= 15.6A
Ipeak= 21.6A

Thames
Irms= 16.5A
Ipeak= 23A
OCP= 27.6

+VGACORE +/- 5%
Countinue current:16.5A
Peak current:23A
OCP minimum 27A



Thames	CNTRL1 GPIO6	CNTRL0 GPIO5	
0.875V	0	0	Ra --> 15K-ohm
0.9V	1	0	Rb --> 10K-ohm
1.0V	1	1	default

Seymour	CNTRL1 GPIO6	CNTRL0 GPIO5	
0.9V	0	0	
1.05V	1	0	
1.15V	1	1	default

[2,6,7,8,9,10,12,13,14,16,21,22,23,24,25,26,27,28,29,34,36,38] +3V
+3V_GFX
[10,26,27,31,32,33,34,35,36,37,38,39] +5VS5
[18] +VGACORE
[21,27,30,31,32,34,37,38,39] +VIN

NB5

PROJECT : LGx MUXLESS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VGACORE (RT8208)	2A

Date: Wednesday, March 07, 2012 | Sheet 40 of 42