IP Core Generator: Multiplier

Features

- Multiplier – Serial Parallel
- Multiplier – Signed
- Multiplier – Signed, Pipeline x 1
- Multiplier – Unsigned
- Multiplier – Unsigned, Pipeline x 1
- Accessible from the Macro Generator Dialog and HDLPlanner™ – Included in IDS for FPGA Devices and System Designer™ for AT94K FPSLIC™ Devices
- Serial Parallel Multiplier Only
  - Variable Width of Input Data
  - Input Representation Selection
  - Clock Inversion Capability
  - Initialization Polarity Selection
- Signed Multiplier Only
  - Variable Width of Input DataA
  - Variable Width of Input DataB
- Signed Multiplier, Pipeline x 1 Only
  - Variable Width of Input DataA
  - Variable Width of Input DataB
  - Initialization Polarity Selection
  - Initialization Selection
- Unsigned Multiplier Only
  - Variable Width of Input DataA
  - Variable Width of Input DataB
  - Output Pins Truncation
- Unsigned Multiplier, Pipeline x 1 Only
  - Variable Width of Input DataA
  - Variable Width of Input DataB
  - Initialization Polarity Selection
  - Initialization Selection

Programmable SLI

AT40K

AT40KAL

AT94K

Application Note

Rev. 2440A–12/01

Multiplier – Serial Parallel

The Serial-parallel Multiplier (SPM) generator can be used to create a signed or unsigned serial by parallel multiplier with serial output. A width *n* unsigned multiplier is constructed in the FPGA by stringing *n* Carry-Save Adders. A width *n* signed multiplier is constructed by stringing n-1 Carry-Save Adders and a two's complement together.

Let X and Y be the n-bit and m-bit number respectively. The parallel input X is multiplied by each bit of serial input with the least significant bit coming first, and each of those partial products is added to the shifted accumulation of the previous product. The serial output is then taken from the output of the least significant bit adder. The output bit has the same weight as the previous serial input bit, and the number of bits in the output is equal to the sum of the number of bits in each of the inputs.

Thus the product[1] is:

$$\{Y\_(m - 1)\} * \{X\_(n - 1) * 2^{(n - 1)} + X\_(n - 2) * 2^{(n - 2)} + ... + X\_(0)\}$$
$$+ \{Y\_(m - 2)\} * \{X\_(n - 1) * 2^{(n - 1)} + X\_(n - 2) * 2^{(n - 2)} + ... + X\_(0)\}$$
$$+ ...$$
$$+ \{Y\_(0)\} * \{X\_(n - 1) * 2^{(n - 1)} + X\_(n - 2) * 2^{(n - 2)} + ... + X\_(0)\}$$

Note: 1. The multiplier uses an asynchronous initialization scheme. After each multiplication operation is complete, the reset pin should be asserted for one clock cycle. This flushes the carry-save registers and is required for correct operation of the multiplier.

Parameters

Parameter	Value	Explanation
Width	Integer > 1	Width of parallel input data
Representation	Signed	Treat Inputs as signed
	Unsigned	Treat inputs as unsigned
Invert Clock	Boolean	Invert the clock input
Initialization Polarity = Low	Boolean	Reset input is active low

Pins

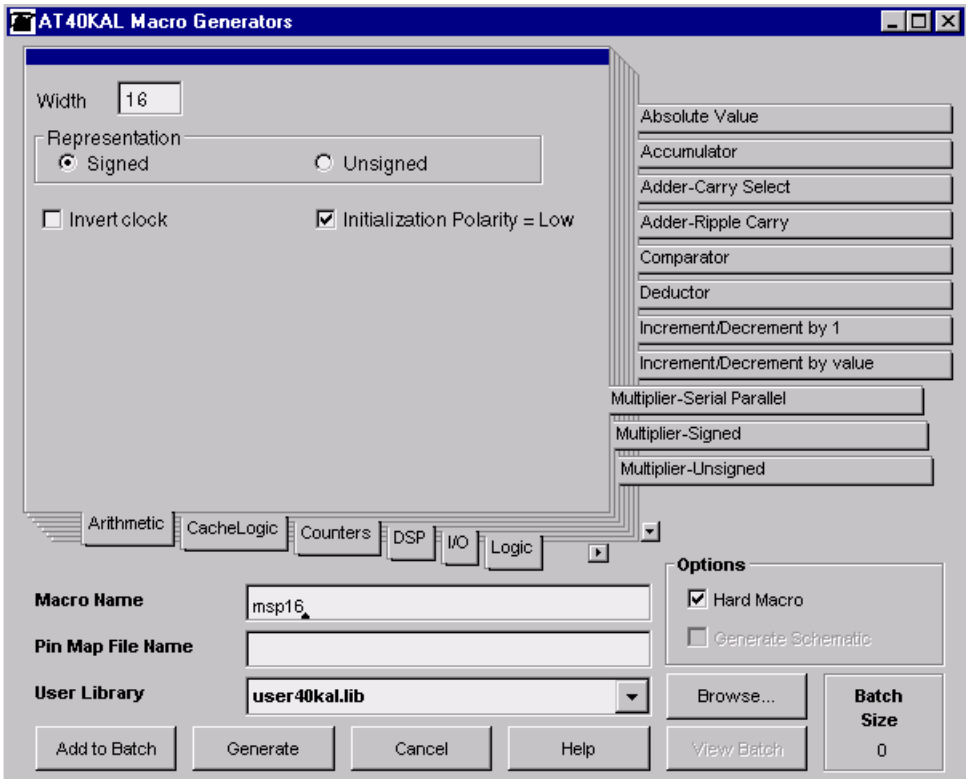
Type	Name	Option	Explanation
In	X[Width - 1:0]	No	Multiplier (parallel input)
In	Y	No	Multiplicand (serial input)
In	R/RN	No	Reset input (active high/low)
Out	PROD	No	Product of x and y (serial output)

Statistics

Device	Name	Speed (MHz)	Delay (ns)	Cells	Size (x * y)
AT40K	msp16	121.8	8.2	32	2 x 16
AT40K	msp8	121.8	8.2	16	2 x 8
AT94K/ AT40KAL	msp16	108.3	9.2	32	2 x 16
AT94K/ AT40KAL	msp8	108.3	9.2	16	2 x 8

Figure 1 shows an example of the msp16 macro options.

Figure 1. Multiplier – Serial Parallel Generator



Multiplier – Signed

The Signed-multiplier generator can be used to generate the product of two varying width inputs. The function it produces is the following:

Product = DATAA * DATAB

where DATAA and DATAB are treated as two's complement signed numbers.

Parameters

Parameter	Value	Explanation
WidthA	Integer > 2	Width of input DataA
WidthB	Integer > 2	Width of input DataB

Pins

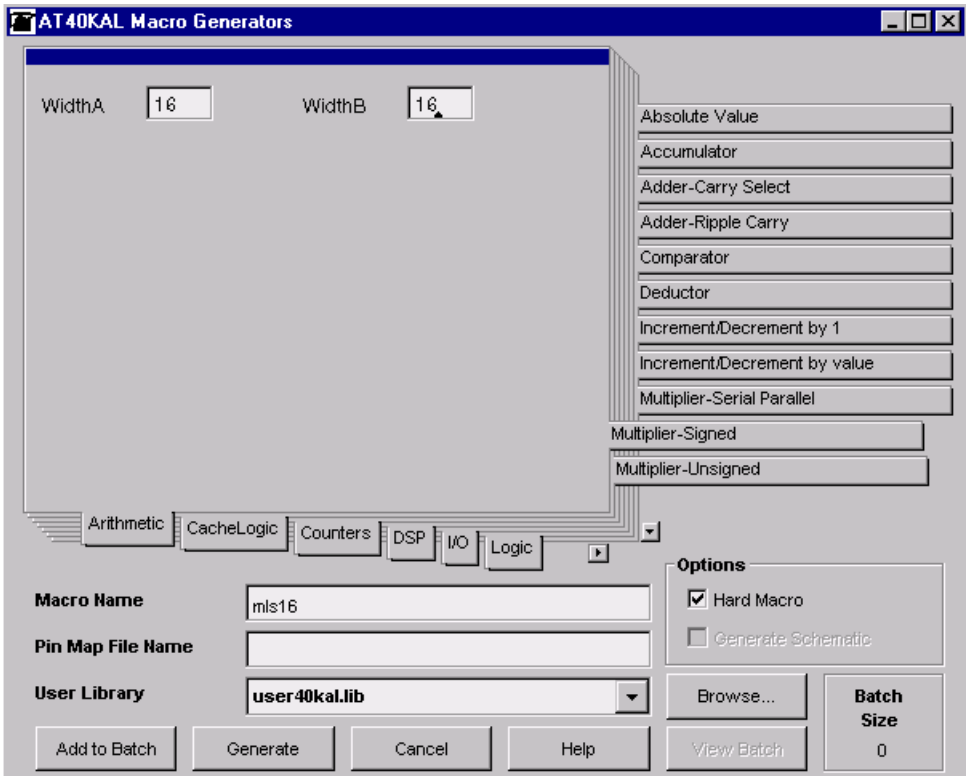
Type	Name	Option	Explanation
In	DATAA[WidthA - 1:0]	No	Multiplicand
In	DATAB[WidthB - 1:0]	No	Multiplier
Out	PRODUCT[Width - 1:0]	No	DataA * DataB (Width is WidthA + WidthB)

Statistics

Device	Name	Speed (MHz)	Delay (ns)	Cells	Size (x * y)
AT40K	mls16	15.5	64.3	289	17 x 17
AT40K	mls8	30.0	33.4	81	9 x 9
AT94K/ AT40KAL	mls16	22.2	45.1	289	17 x 17
AT94K/ AT40KAL	mls8	40.8	24.5	81	9 x 9

Figure 2 shows an example of the mls16 macro options.

Figure 2. Multiplier – Signed Generator



Multiplier – Signed, Pipeline x 1

This component can be used to generate the product of two varying width inputs. A single stage of pipelining is used to produce a considerably faster macro than the standard signed multiplier with minimal additional logic.

The function it produces is the following:

Product = DATAA * DATAB

where DATAA and DATAB are treated as two's complement signed numbers.

Parameters

Parameter	Value	Explanation
WidthA	Integer > 2	Width of input DataA
WidthB	Integer > 2	Width of input DataB
Invert Clock	Boolean	Invert the clock input
Initialization Polarity = Low	Boolean	Reset input is active low
Initialization	Reset	Provide a reset input for initialization of the pipeline registers
	None	Pipeline registers are automatically initialized on power-up

Pins

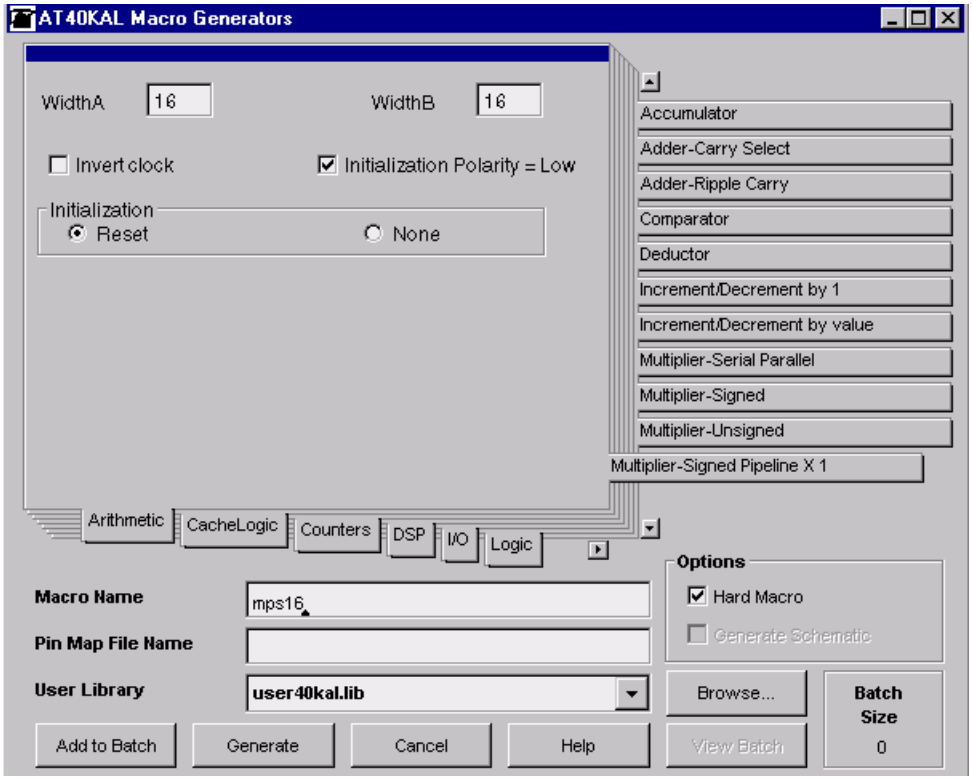
Type	Name	Option	Explanation
In	DATAA[WidthA - 1:0]	No	Multiplicand
In	DATAB[WidthB - 1:0]	No	Multiplier
In	CLK/CLKN	No	Clock input (noninverted/inverted)
In	R/RN	Yes	Reset input (active high/low)
Out	PRODUCT[Width - 1:0]	No	DataA * DataB (Width is WidthA + WidthB)

Statistics

Device	Name	Speed (MHz)	Delay (ns)	Cells	Size (x * y)
AT40K	mps16	24.9	40.1	306	17 x 18
AT40K	mps8	44.7	22.4	90	9 x 10
AT94K/ AT40KAL	mps16	33.8	29.6	306	17 x 18
AT94K/ AT40KAL	mps8	68.6	14.6	90	9 x 10

Figure 3 shows an example of the mps16 macro options.

Figure 3. Multiplier – Signed Pipeline x 1 Generator



Multiplier – Unsigned

The Unsigned-multiplier generator can be used to generate the product of two varying width inputs. The function it produces is the following:

Product = DATAA * DATAB

Where DATAA and DATAB are treated as unsigned numbers.

Parameters

Parameter	Value	Explanation
WidthA	Integer > 2	Width of input DataA
WidthB	Integer > 2	Width of input DataB
Truncate Result to n Least Significant Bits	Integer ≥ 0	The number of output pins that have to be included in the layout starting from the LSB. This option saves the layout area by not including the unnecessary output pins. If this value is left at 0, all outputs will be present.

Pins

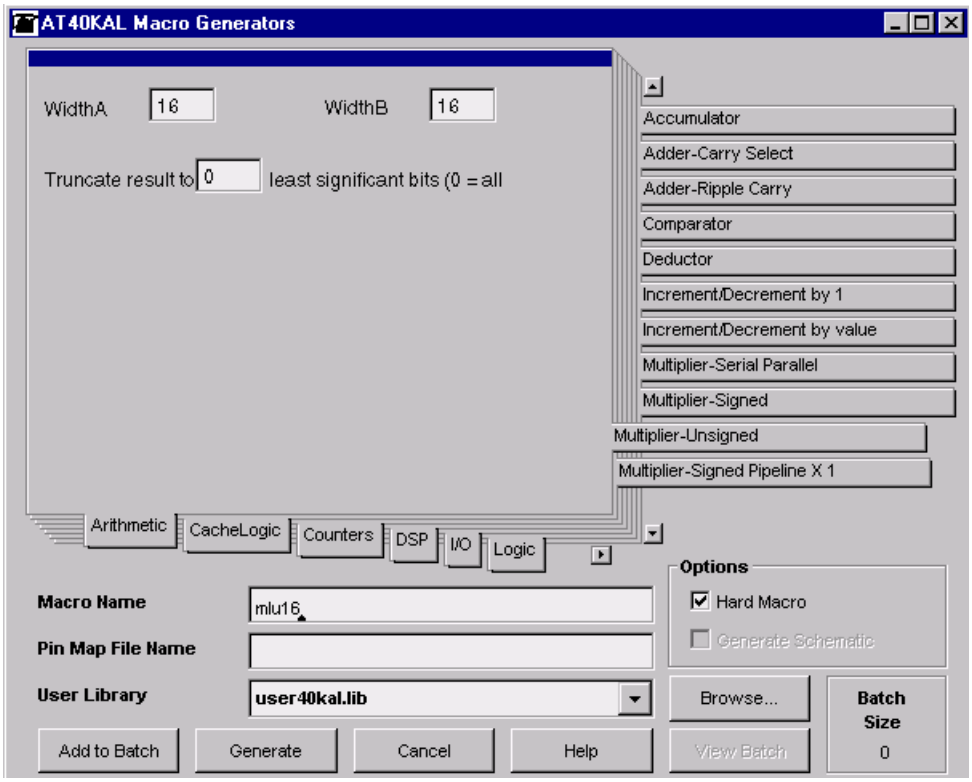
Type	Name	Option	Explanation
In	DataA[WidthA - 1:0]	No	Multiplicand
In	DataB[WidthB - 1:0]	No	Multiplier
Out	PRODUCT[Width - 1:0]	No	DataA * DataB (Width is WidthA + WidthB)

Statistics

Device	Name	Speed (MHz)	Delay (ns)	Cells	Size (x * y)
AT40K	mlu16	16.0	62.7	256	16 x 16
AT40K	mlu8	31.5	31.7	64	8 x 8
AT94K/ AT40KAL	mlu16	22.8	43.8	256	16 x 16
AT94K/ AT40KAL	mlu8	42.9	23.3	64	8 x 8

Figure 4 shows an example of the mlu16 macro options.

Figure 4. Multiplier – Unsigned Generator



Multiplier – Unsigned, Pipeline x 1

This component can be used to generate the product of two varying width inputs. A single stage of pipelining is used to produce a considerably faster macro than the standard unsigned multiplier with minimal additional logic.

The function it produces is the following:

Product = DATAA * DATAB

Where DATAA and DATAB are treated as unsigned numbers.

Parameters

Parameter	Value	Explanation
WidthA	Integer > 2	Width of input DataA
WidthB	Integer > 2	Width of input DataB
Invert Clock	Boolean	Invert the clock input
Initialization Polarity = Low	Boolean	Reset input is active low
Initialization	Reset	Provide a Reset Input for Initialization of the Pipeline Registers
	None	Pipeline Registers are Automatically Initialized on Power-up

Pins

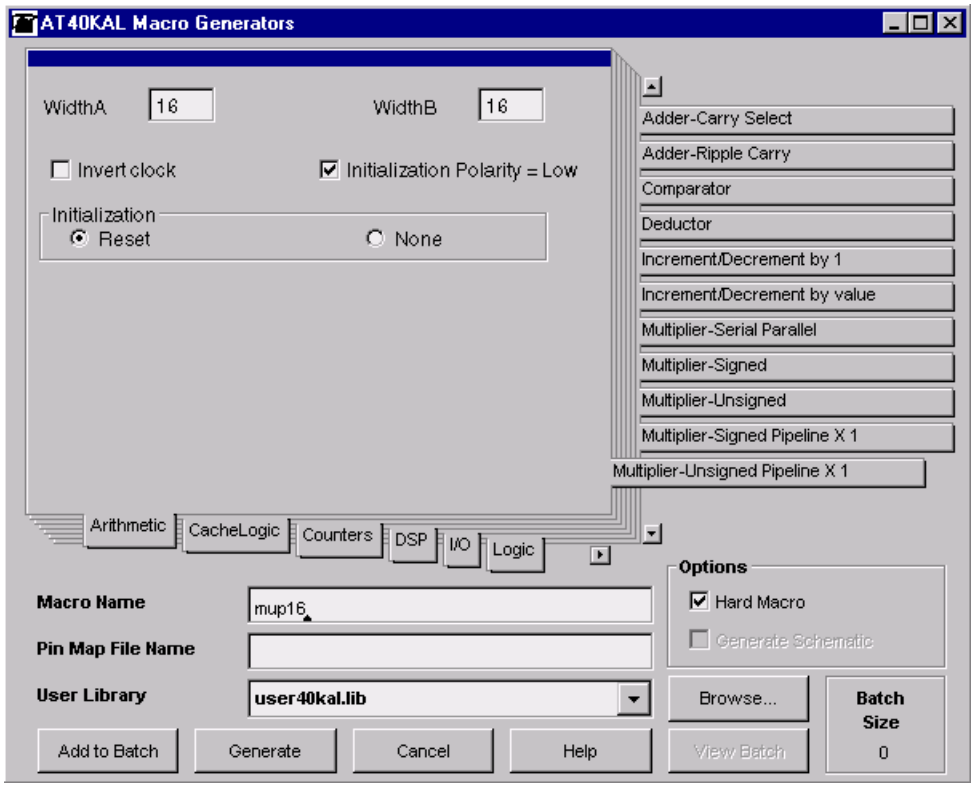
Type	Name	Option	Explanation
In	DATAA[WidthA - 1:0]	No	Multiplicand
In	DATAB[WidthB - 1:0]	No	Multiplier
In	CLK/CLKN	No	Clock input (noninverted/inverted)
In	R/RN	Yes	Reset input (active high/low)
Out	PRODUCT[Width - 1:0]	No	DataA * DataB (Width is WidthA + WidthB)

Statistics

Device	Name	Speed (MHz)	Delay (ns)	Cells	Size (x * y)
AT40K	mup16	27.3	36.7	272	16 x 17
AT40K	mup8	52.9	18.9	72	8 x 9
AT94K/ AT40KAL	mup16	38.7	25.8	272	16 x 17
AT94K/ AT40KAL	mup8	84.9	11.8	72	8 x 9

Figure 5 shows an example of the mup16 macro options.

Figure 5. Multiplier – Unsigned Generator



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